AFSC5G23D37 2300-2400 MHz REFERENCE CIRCUIT

ORDERABLE PART NUMBER: **AFSC5G23D37-EVB**

PUBLIC

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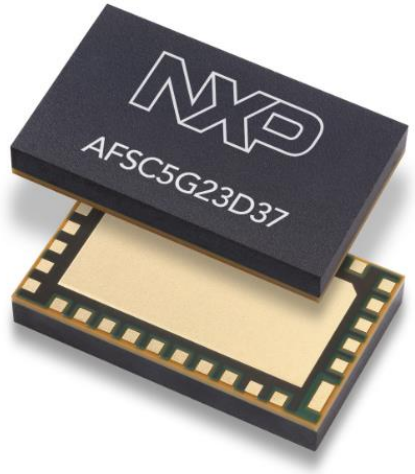
Introduction

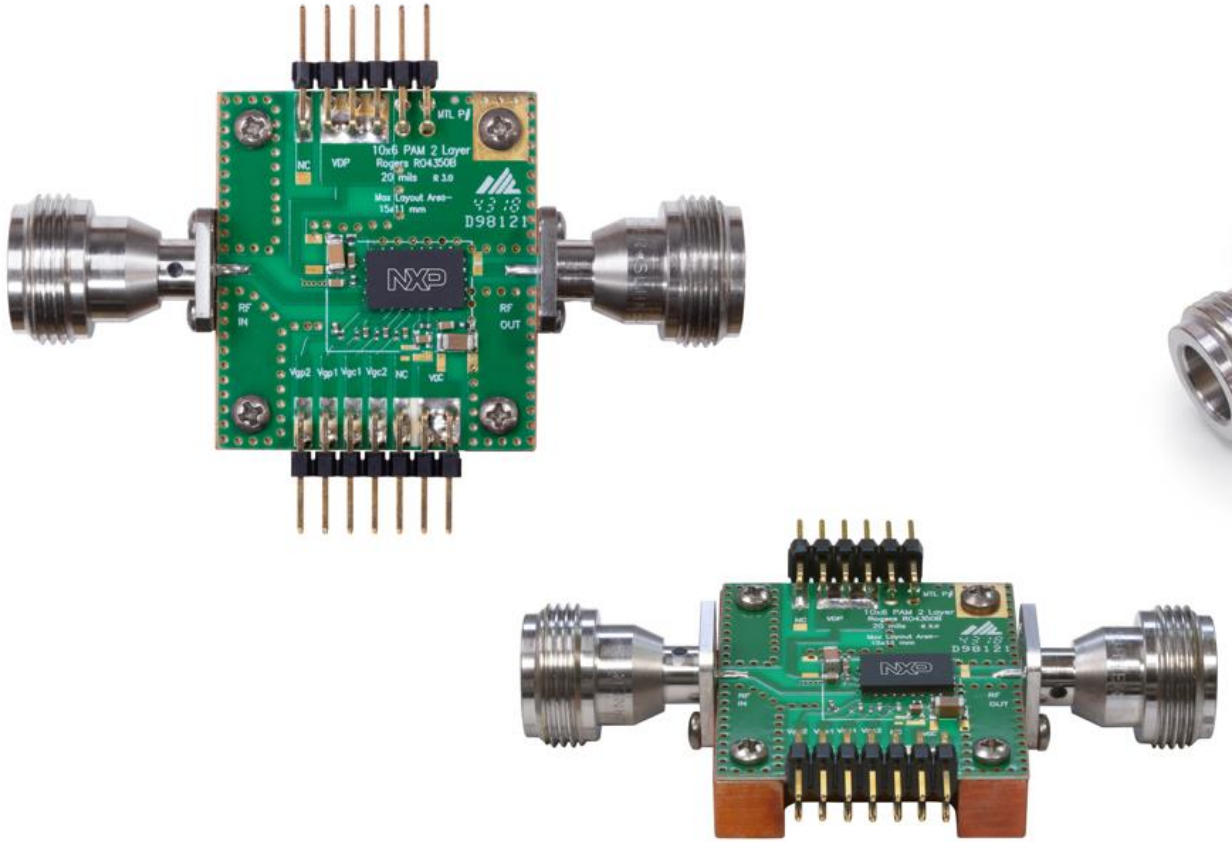
- The NXP AFSC5G23D37 is a 2300-2400 MHz, 5 W average RF power multi-chip module housed in a 10 mm x 6 mm LGA package. Its 50 ohm fully matched input and output ensures a small PA footprint.
  - Further details about the device, including its data sheet, are available here.

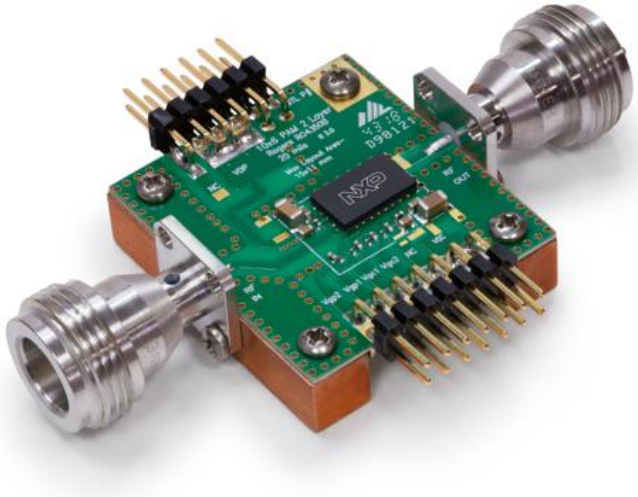
- The following pages describe the 2300-2400 MHz reference circuit.
  Its typical application is 5G 64T64R mMIMO active antenna systems for cellular base stations.

- The reference circuit can be ordered through NXP's distribution partners and etailers using part number AFSC5G23D37-EVB.



Circuit Overview – 3.30 cm × 3.71 cm (1.30″ × 1.46″)





Typical Performance 1/2

Typical LTE Performance: P_{out} = 5 W Avg., 1 x 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
2300 MHz	26.7	–29.4	38.4
2355 MHz	27.0	–30.9	37.9
2400 MHz	27.1	–31.2	37.0

Operating conditions: V_{DDc} = V_{DDp} = 26 Vdc, I_{DQc1} = 24 mA, I_{DQc2} = 45 mA, V_{GGp1} = 1.7 Vdc, V_{GGp2} = 1.4 Vdc
All data measured in fixture with device soldered in reference circuit.

Typical Performance 2/2

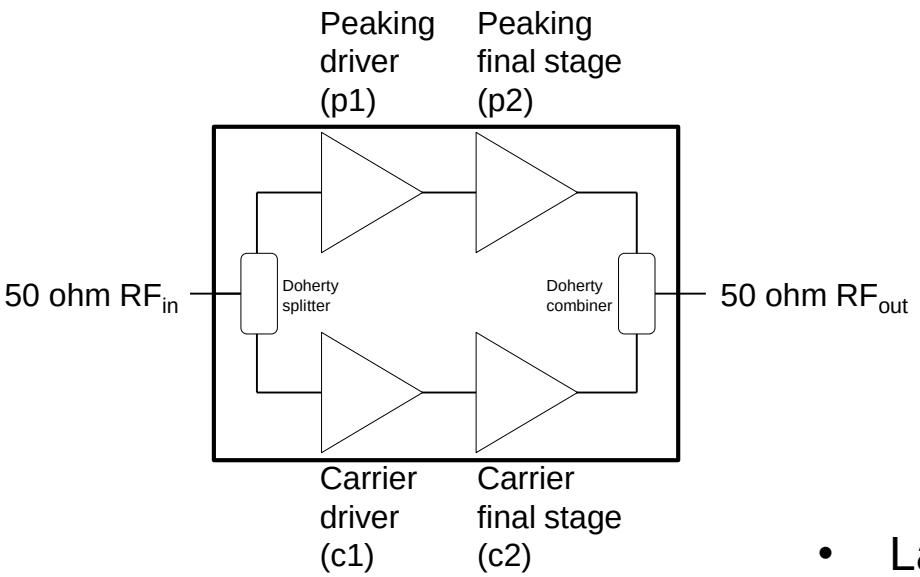
Operating conditions: V_{DDc} = V_{DDp} = 26 Vdc, I_{DQc1} = 24 mA, I_{DQc2} = 45 mA, V_{GGp1} = 1.7 Vdc, V_{GGp2} = 1.4 Vdc, P_{out} = 5 W Avg., 2355 MHz

VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Quiescent Current Accuracy over Temperature (5) with 2.2 kΩ Gate Feed Resistors (–40 to 85°C) Stage 1 with 2.2 kΩ Gate Feed Resistors (–40 to 85°C) Stage 2	ΔI_{QT}	— —	1.0 2.0	— —	%
1-carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	27.0	—	dB
Power Added Efficiency	PAE	—	37.9	—	%
Adjacent Channel Power Ratio	ACPR	—	–30.9	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–38.0	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–43.9	—	dBc
Output Peak-to-Average Ratio @ 0.01% Probability	PAR	—	7.4	—	dB
Gain Flatness (6)	G_F	—	0.4	—	dB
Fast CW, 27 ms Sweep					
P_{out} @ 3 dB Compression Point	P3dB	—	44.5	—	dBm
AM/PM @ P3dB	Φ	—	–18	—	°
Pulsed CW, 10 µsec(on), 10% Duty Cycle @ P1dB					
Gain Variation over Temperature (–40°C to +105°C)	ΔG	—	0.033	—	dB/°C
Output Power Variation over Temperature (–40°C to +105°C)	ΔP1dB	—	0.013	—	dB/°C

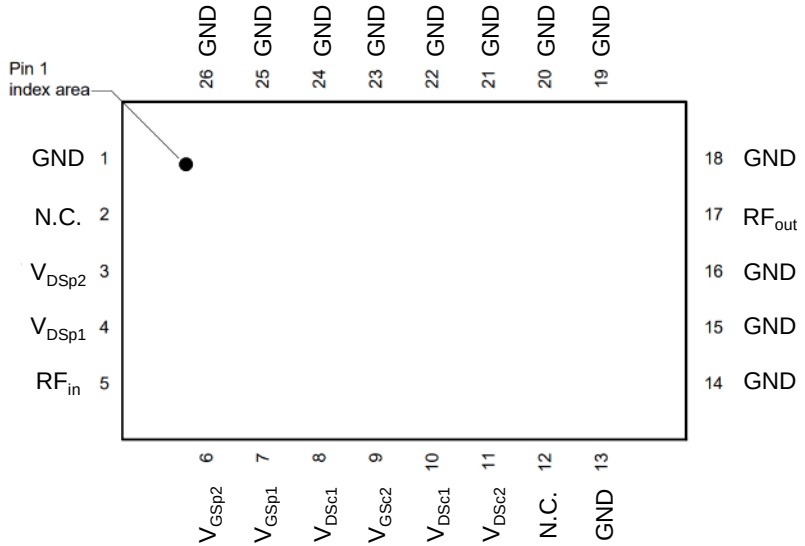
All data measured in fixture with device soldered in reference circuit.

Component Connection Details

- Functional Block Diagram:



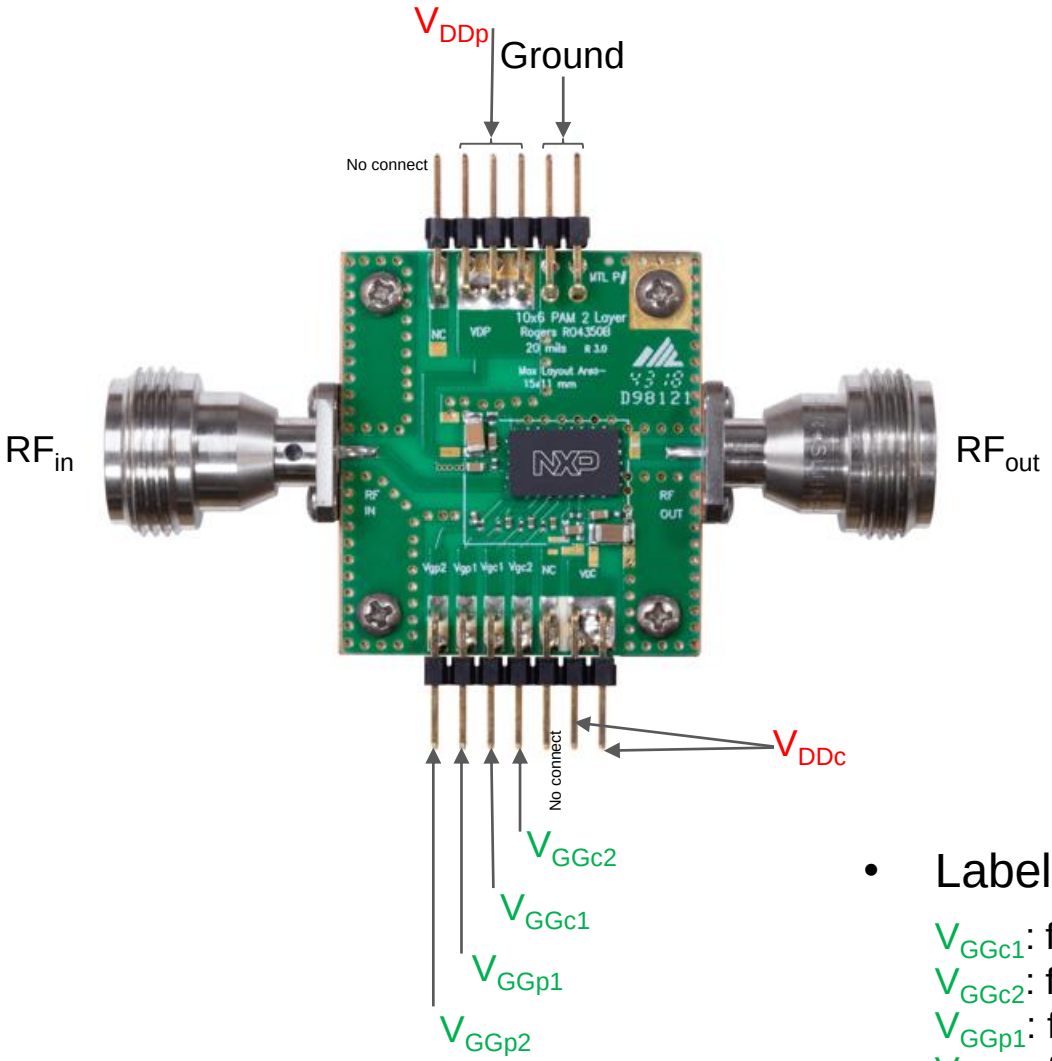
- Pin Connections (top view):

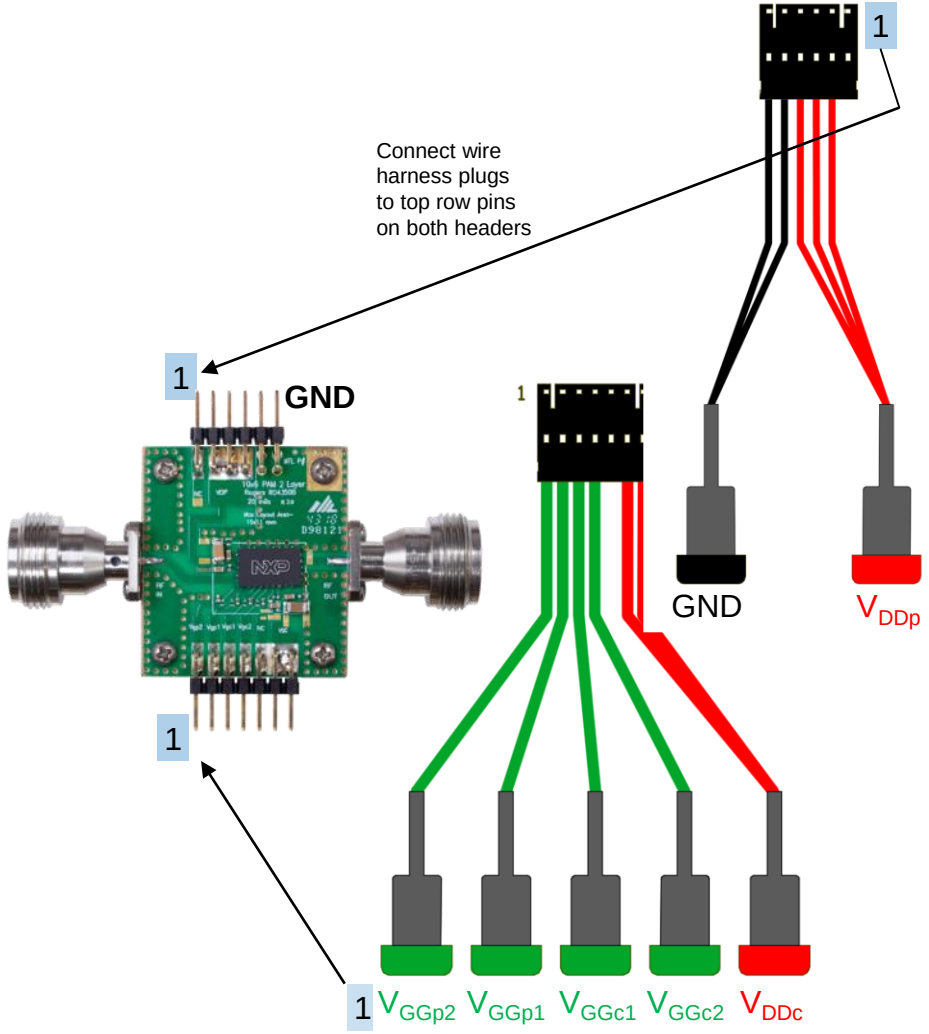


- Labeling:

V_{GSc1}: gate voltage for carrier driver
V_{GSc2}: gate voltage for carrier final stage
V_{GSp1}: gate voltage for peaking driver
V_{GSp2}: gate voltage for peaking final stage
V_{DSc1}: drain voltage for carrier driver
V_{DSc2}: drain voltage for carrier final stage
V_{DSp1}: drain voltage for peaking driver
V_{DSp2}: drain voltage for peaking final stage
I_{DQc1}: quiescent current for carrier driver
I_{DQc2}: quiescent current for carrier final stage
V_{DSc2} and V_{DSp2} are DC coupled internal to the package

Reference Circuit Connection Details



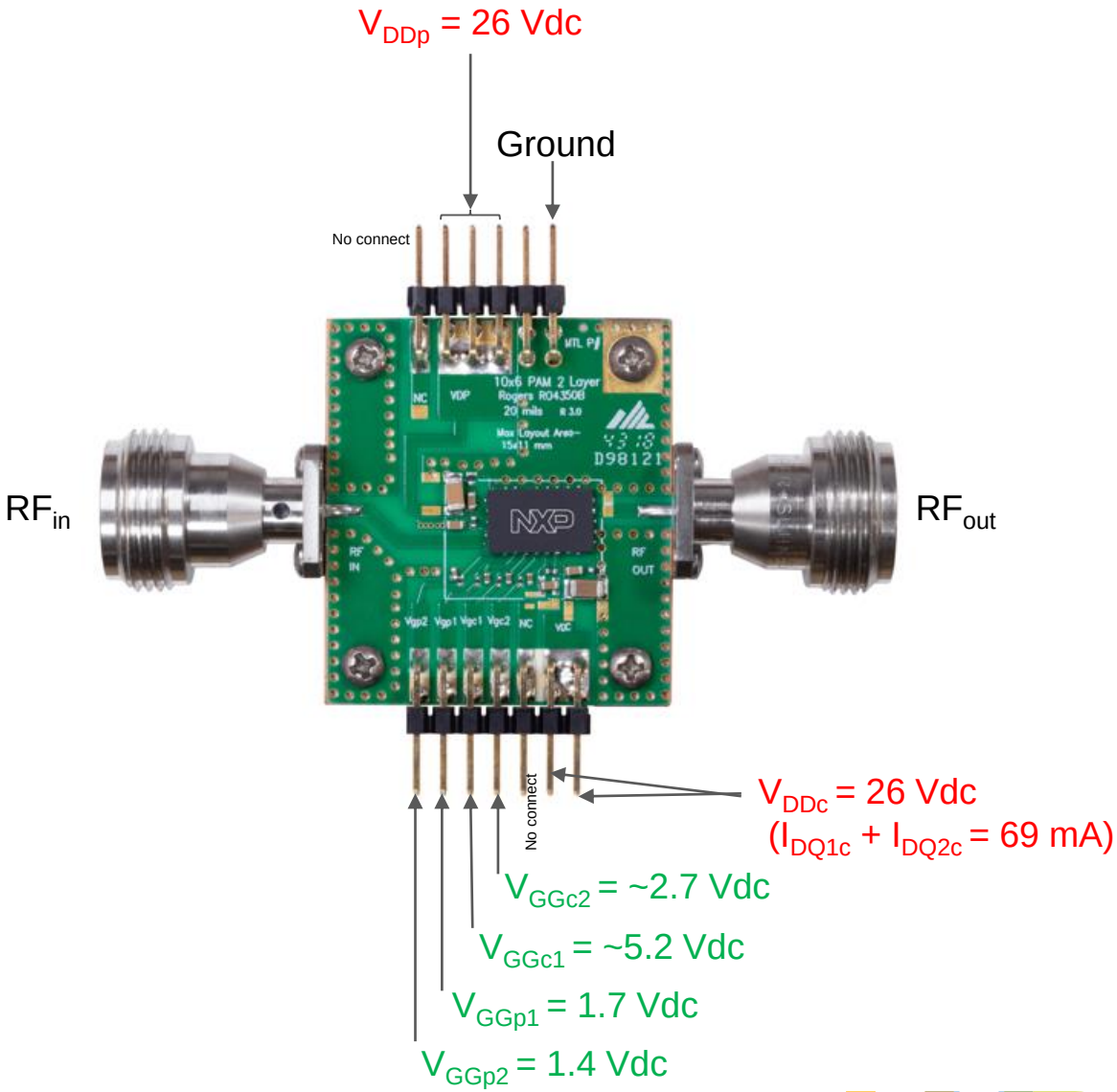


- Labeling:

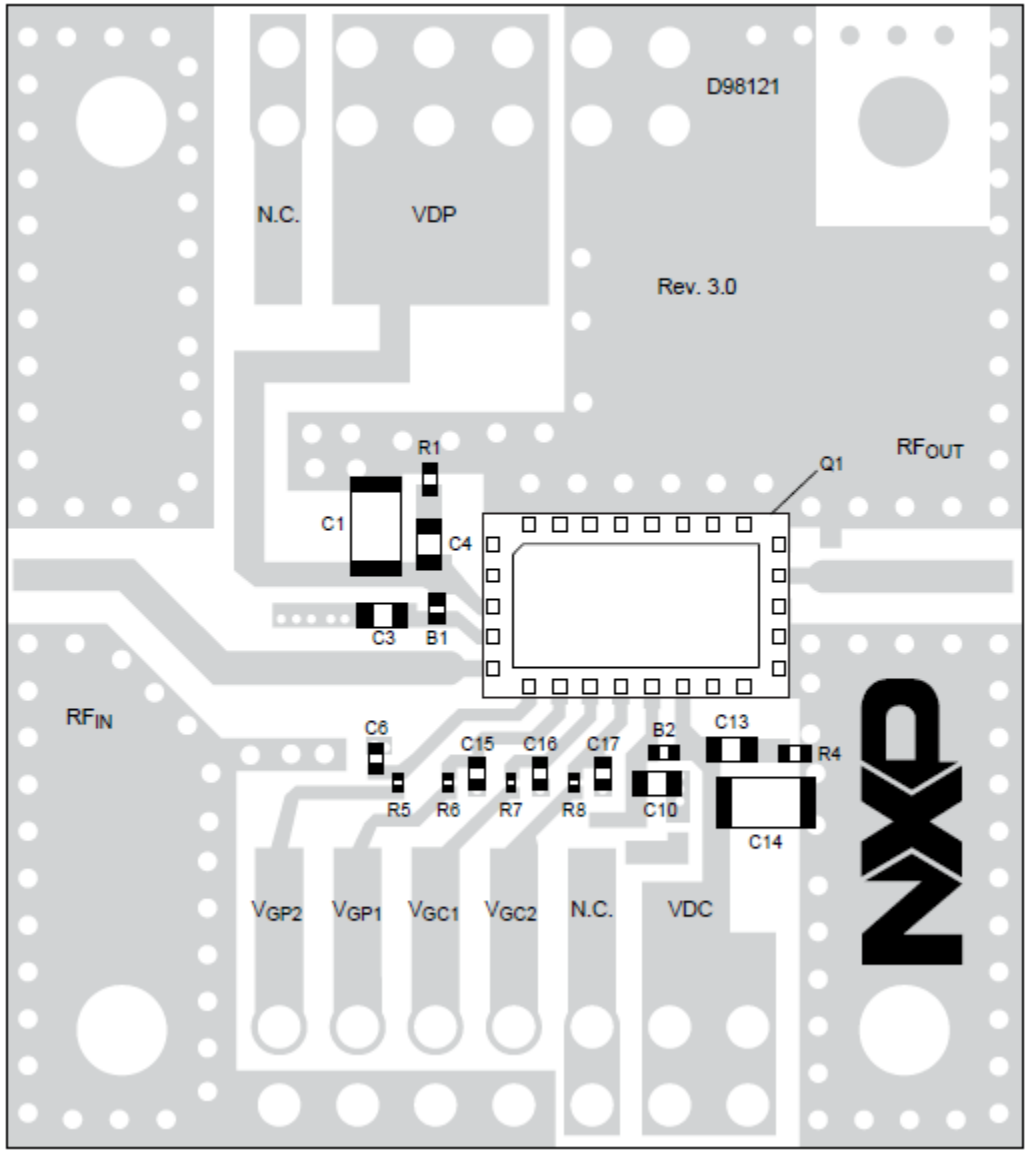
V_{GGc1}: fixture gate voltage for carrier driver
V_{GGc2}: fixture gate voltage for carrier final stage
V_{GGp1}: fixture gate voltage for peaking driver
V_{GGp2}: fixture gate bias voltage for peaking final stage
V_{DDc}: fixture drain voltage for both V_{DSc1} and V_{DSc2}
V_{DDp}: fixture drain voltage for both V_{DSp1} and V_{DSp2}

Quick Start

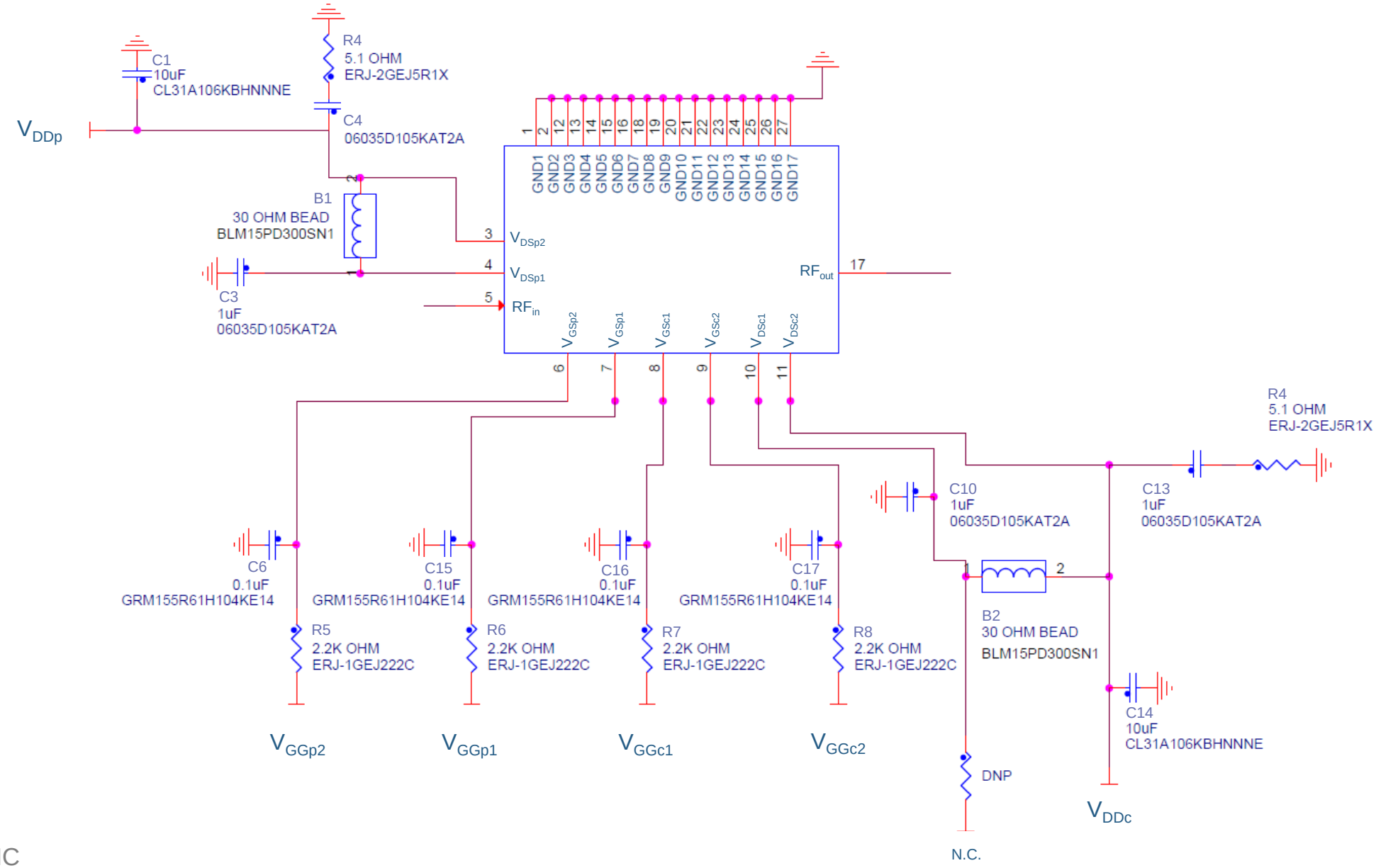
1. Mount the reference circuit onto a heatsink capable of dissipating more than 8 W in order to provide enough thermal dissipation (the baseplate included in this reference circuit is not sufficient to serve as a standalone heatsink).
2. Connect the ground.
3. Terminate the RF output with a 50 ohm load capable of handling more than 36 W peak power.
4. Connect the RF input to a 50 ohm source with the RF off.
5. Connect the carrier drain voltage (V_{DDc}) and the peaking drain voltage (V_{DDp}) and raise them slowly to 26 V in no particular order. Current should be 0 A.
6. Connect the gate voltage for the carrier driver (V_{GGc1}) and raise it slowly to the typical carrier driver's quiescent current of I_{DQc1} = 24 mA. V_{GGc1} should be around 5.2 V.
7. Set V_{GGc1} to 0 V. Connect the gate voltage for the carrier final stage (V_{GGc2}) and raise it slowly to the carrier final stage's quiescent current of I_{DQc2} = 45 mA. V_{GGc2} should typically be around 2.7 V.
8. Set V_{GGc1} and V_{GGc2} to the values found in steps 6 and 7. The total quiescent current I_{DQc1} + I_{DQc2} should be around 69 mA.
9. Set V_{GGp1} at 1.7 V and V_{GGp2} at 1.4 V.
10. Raise the RF input slowly to 10 mW (10 dBm).
11. Check the RF output power (typically 5 W avg), the drain current (around 0.5 A for this power level) and the temperature of the board.



Component Placement Reference



Schematics


C1
10uF
CL31A106KBHNNNE
R4
5.1 OHM
ERJ-2GEJ5R1X
C4
06035D105KAT2A
VDDp
B1
30 OHM BEAD
BLM15PD300SN1
C3
1uF
06035D105KAT2A
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
VDSp2
VDSp1
RFin
RFout
VGSp2
VGSp1
VGSc1
VGSc2
VDSc1
VDSc2
C6
0.1uF
GRM155R61H104KE14
C15
0.1uF
GRM155R61H104KE14
C16
0.1uF
GRM155R61H104KE14
C17
0.1uF
GRM155R61H104KE14
R5
2.2K OHM
ERJ-1GEJ222C
R6
2.2K OHM
ERJ-1GEJ222C
R7
2.2K OHM
ERJ-1GEJ222C
R8
2.2K OHM
ERJ-1GEJ222C
VGGp2
VGGp1
VGGc1
VGGc2
C10
1uF
06035D105KAT2A
R4
5.1 OHM
ERJ-2GEJ5R1X
C13
1uF
06035D105KAT2A
B2
30 OHM BEAD
BLM15PD300SN1
C14
10uF
CL31A106KBHNNNE
DNP
N.C.
VDDc

Bill of Materials

Part	Description	Part Number	Manufacturer
B1, B2	30 Ω Ferrite Bead	BLM15PD300SN1	Murata
C1, C14	10 μF Chip Capacitor	CL31A106KBHNNNE	Samsung
C3, C4, C10, C13	1 μF Chip Capacitor	06035D105KAT2A	AVX
C6, C15, C16, C17	0.1 μF Chip Capacitor	GRM155R61H104KE14	Murata
Q1	Power Amplifier Module	AFSC5G23D37	NXP
R1, R4	5.1 Ω, 1/10 W Chip Resistor	ERJ-2GEJ5R1X	Panasonic
R5, R6, R7, R8	2.2 kΩ, 1/20 W Chip Resistor	ERJ-1GEJ222C	Panasonic
PCB	Rogers RO4350B, 0.020″, ε_r = 3.67	D98121	MTL

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.

Revision History

- The following table summarizes revisions to the content of the AFSC5G23D37 2300-2400 MHz Reference Circuit zip file.

Revision	Date	Description
0	September 2019	• Initial Release

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