Freescale Semiconductor
56F8155 Product Brief

The 56F8155 designers subscribe to the philosophy that you can never have enough of a good thing. That is why they added more on-chip Flash memory (up to 272KB), Analog-to-Digital Converter inputs, timer channels, and added a PWM and a Quadrature Decoder to the peripherals found in smaller members of the device family. With these additions, a whole new set of applications can now benefit from the hybrid MCU/DSP capabilities of the 56800E architecture.

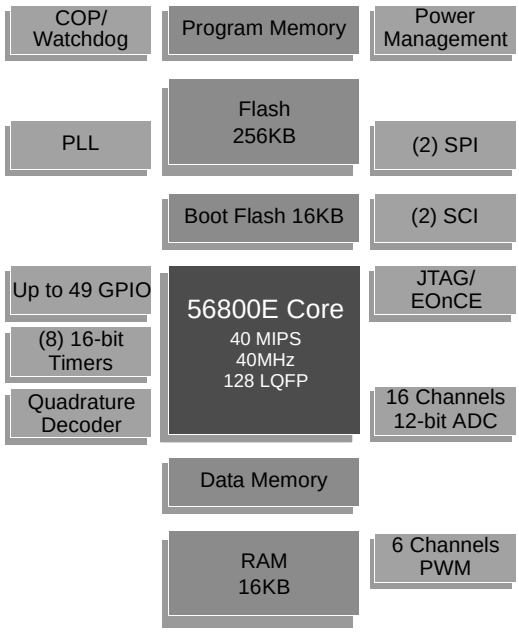
Imagine adding signal processing capabilities to a smart user interface, or adding sophisticated communication protocol to an industrial control application. The possibilities are endless, especially when you consider that you can have access to all these advanced features at extended temperatures.

BENEFITS

- Hybrid architecture facilitates implementation of both control and signal processing functions in a single device
- High-performance, secured Flash memory eliminates the need for external storage devices
- Extended temperature range up to 105ºC allows for operation of non-volatile memory in industrial applications
- Flash memory emulation of EEPROM eliminates the need for external non-volatile memory
- 32-bit performance with 16-bit code density
- On-chip voltage regulator and power management reduces overall system cost
- Diversity of peripheral configuration facilitates the elimination of external components, improving system integration and reliability
- This device boots directly from Flash, providing additional application flexibility
- High-performance PWM with programmable fault capability simplifies design and promotes compliance with safety regulations
- PWM and ADC modules are tightly coupled to reduce processing overhead
- Low-voltage interrupts protect the system from brownout or power failure
- Simple in-application Flash memory programming via Enhanced OnCE™ or serial communication

56800E CORE FEATURES

- Up to 40 MIPS at a guaranteed 40MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging
- Four 36-bit accumulators
- 16- and 32-bit bidirectional barrel shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops available
- Three internal address buses
- Four internal data buses
- Architectural support for 8-, 16-, and 32-bit single-cycle data fetches
- MCU-style software stack support
- Controller-style addressing modes and instructions
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Proven to deliver more control functionality with a smaller memory footprint than competing architectures



EXAMPLE APPLICATIONS

- Polyphase metering
- UPS
- Electric vehicles
- Currency validation
- Industrial control/networking
- Home appliances
- Smart sensors
- Fire and security systems
- Medical monitoring

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MEMORY FEATURES

- Architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory includes high-speed volatile and non-volatile components
  - 256KB of Program Flash
  - 16KB of Data RAM
  - 16KB of Boot Flash
- All memories operate at 40MHz (zero wait states) over temperature range (-40° to +105°C), with no software tricks or hardware accelerators required
- Flash security feature prevents unauthorized accesses to its content

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

56F8155 PERIPHERAL CIRCUIT FEATURES

- Pulse Width Modulator (PWM) module with six outputs and four programmable fault inputs
- Two Serial Peripheral Interfaces (SPI)
- Two Serial Communication Interfaces (SCI)
- Eight 16-bit Timers with input and output compare capability
- Four-input Quadrature Decoder
- On-chip 3.3V to 2.6V voltage regulator
- Software-programmable Phase Lock Loop (PLL)
- 12-bit Analog-to-Digital Converters (ADC) with 16 inputs, self calibration, and current injection capability
- Up to 49 General Purpose I/O (GPIO) pins
- External reset input pin for hardware reset
- Computer Operating Properly (COP)
- Integrated Power-On Reset and Low-Voltage Interrupt module
- I^2C Communications Master Mode (emulated)

ORDERING INFORMATION

PART	***MC56F8155***
PACKAGE	***128 LQFP***
ORDER NUMBER	***MC56F8155VFG***
TEMPERATURE RANGE	***-40° to 105°C***

PRODUCT DOCUMENTATION

56F8300 Peripherals Manual	Detailed peripheral description of the 56F8300 family of devices Order Number: MC56F8300UM
56F8355 / 56F8155 Technical Data Sheet	Electrical and timing specifications, device-specific peripheral information and package and pin descriptions Order Number: MC56F8355
56F8155 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces Order number: MC56F8155PB
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit core processor and the instruction set Order Number: DSP56800ERM

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MC56F8155PB