MOTOROLA

Microprocessor and Memory Technologies Group

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MC68SC302

Errata and Added Information to

MC68SC302 Passive ISDN Protocol Engine User's Manual

May 23, 1997

New items in *italics*

4.4.2 SERIAL INTERFACE MASK REGISTER (SIMASK)

On page 4-14, SIMASK description the SC302 UM says: "...The serial data strobes, SDS1 and SDS2 are asserted for the entire 8 bit time slot independent of the setting of the bits in the SIMASK register"

The UM should say: "...The serial data strobes, SDS1 and SDS2 are asserted for the bits which are set in the associated B channel mask, and negated for the bits which are cleared in the SIMASK register"

~~4.5.3.2.3 Mixed Address EEPROM.~~

~~On page 4-52, update "The 93C46 in the "by 8" organization is an example of this type of EEPROM" to:~~

~~The SGS-THOMSON 93C46A and the Xicor X25020 in the "by 8" organization are examples of this type of EEPROM.~~

5.4.1 Resource Data Layout in a Byte Serial Device

1. On page 5-7, change Table 5-3 Resource Data Layout as follows:

ADDRESS	NAME	REGISTER-DESTINATION
0x00-01	Serial EEPROM Type/Mode	-

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ADDRESS	NAME	REGISTER-DESTINATION
0x02-03	Reserved for future use. Must be programmed to 0	-
0x04	Serial EEPROM Type	-
0x05-06	Reserved for future use. Must be programmed to 0	-
0x07	Implementation Specific Information	0x22
0x08	First bye of Standard Resource Data	-

2. On page 5-9, Figure 5-5. ISA-PNP Resource Data Layout in a Byte Serial EEPROM Device, the words “Serial Number” next to Byte 3 should be moved down one row so that they align with the words Byte 0.

5.4.3 I/O Configuration

On page 5-10, update the following items:

- Byte 0: I/O port descriptor tag (value = 01000111B = 0x47)
- Byte 1: Information byte: SC302 supports 16-bit address decoding, therefore bit 0 = 1, and bits 7 – 1 are reserved and must be 0 (value = 0x01).

5.4.4 Memory Configuration

On page 5-11, update the following items

- Byte 0: 10000001B = 0x81 (Memory Range Descriptor tag).
- Bytes 1-2: Length of the Memory Range Descriptor, bits[7:0] and bits [15:8] (values = 0x09 and 0x00, respectively, giving a length of 0x0009).
- Byte 3: 0_0_0_1_0_0_0_1= 0x11 (Information field: [Reserved]_[Not Expansion ROM]_[Not shadowable]_[8/16-bit supported]_[Decode support Range Length]_[Non-cachable]_[Writable]).

5.5 ISA-PNP CARD LEVEL CONTROL REGISTERS

1. On page 5-17, the ISI register, bit 5 has an error in the note. It should say “LOADED FROM 0x07 IN BYTE SERIAL DEVICE.”

2. On page 5-19, missing closing parentheses: Card Level (Vendor Defined)

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