RESET issue:

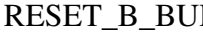
To reset the HDD, the level shifter buffer needs to be enabled by CS5, and a GPIO used.

- A dummy read or write access with RESET low (GPIO low) could be done if a 25us reset could be achieved. Unfortunately, this is a too long access for the memory controller. => not a solution.
- Simply, the CS5 could be controlled manually as a simple GPIO to enable the buffer for enough time. Actually, the RW signal default level enables the buffers direction from HDD to processor. Then, there is a bus contention in this case, as the bus is not officially used by the memory controller, due to manually controlled CS5. => not a solution.

Conclusion:
There is no software workaround, and a hardware fix should be used. HW workaround could be made with the controlled GPIO and a RC cell (please see below).

HW schematics:

- pull up on DIOR and DIOW are recommended for proper signals shape
- reset with RC cell: +Vcc ----[R]---o---|C|---GND R=10k,C=0.1uF=>T~1ms



DMA access:

In asynchronous mode of the EIM, if the DMAC is not programmed to access the EIM in 16bits, there is an issue.
Intern 32bits access between DMAC and EIM is the only specified. But the following issue appears by the 32bits access splitted into 2x16bits access. Indeed, the data register is at the address 0x10, and the EIM will do 2 accesses at 0x10 then 0x12.
So, 1 by 2 data are wrong, as read at a wrong address.
When the DMA is set to access the EIM in 16bits, all the access are done at the same address, so no problem, but also not allowed.

A HW fix could be to use a simple AND gate between the inverted DMARQ and A1.
A1_gated = ~DMARQ & A1.
Without DMA request, DMARQ=0 => ~DMARQ=1 => A1_gated=A1 as for simple register access.
During a DMA request, DMARQ=1=> ~DMARQ=0 => A1_gated=0 and the address is always 0x10

No SW workaround. In synchronous mode, only the first address is asserted, and then the device incremented by itself, so in our case, only the 0x10 address will be asserted. That is what we would like.

Yet, then the OE and EB signals are asserted during all the burst, as everything is synchronized on BCLK! And these signals toggle no more for each read/write word, whereas the HDD still expect each word to be validated by OE or EB.