Table of Contents

Rev	Data	Revision History	PCB Version
A	02/12/2014	Initial Version	A
A1	02/12/2014	Assign a different agile part number for U38 PMIC, as a new image programmed to the internal OTROM	A
B	23/12/2014	1. Correct DDR data line cross between nibbles issue 2. Replace GPIO2_01,02,03,11&12 with GPIO1_14,18,16, 20&22 3. Connect GPIO1_14 to SW4.3 4. Change U15,U18 VCC to 3.3V as the new GPIO power is 3.3V, move the original caps to the NOR 1.8V and add new two caps as DNP to the 3.3V 5. Change the SW4 pull high voltage to 3.3V as the new GPIO power is 3.3V 6. Connect the U17,U42 address pin to 3.3V 7. Populate R107,R109 8. Set SW4.2 to on 9. Use POR reset to RTL8211 PHY 10. DNP R164 11. Solder Silicon 12. Change SW2 setting to SPI boot	B
C	13/05/2015	1. P6: disconnect IFC_WE_n to SW4.1,add R402 from IFC_WE_n to ground 2. P6: connect IFC_OE_n to SW4.1 3. P6: connect IFC_WP_n to SW4.2 4. P6: change R132 to 330ohm 5. P6: Use IDTQS3VH257PA to switch CS and RB signal 6. P6: reconnect NOR flash use small endian connection 7. P7: change R282 to 49.9ohm for EMI 8. P7: change R155,R156 to 330ohm;add Q29,Q30 for eMMC detect and write protection 9. P8: disconnect GPIO1_18 to SW4.4, add a test point 10. P9: populate C331 for EMI 11. P14: populate C45, change C42 to 22PF and populate, change R50 to 33ohm for EMI 12. P14: add R404 39ohm to divide the 125M clock to 1.8V 13. P14: populate C22,C24 for EMI,delete R41 for EMI 14. P15: populate C20,C23 for EMI 15. P16: DNP J7 16. P19: Delete R103 for EMI;DNP J12 17. P20: DNP J14 18. P21: add C611 fix LDO out 0.5V without enabling issue 19. P22: connect J9.3 to GND 20. P6: Disconnect GPIO2_13,GPIO2_14 to LEDs, add test point to GPIOs. 21. P18. Add LEDs to PCIe slot pin44 22. P9. connect GPIO3_0~GPIO3_3as PCIE wake up and clkreq use GPIO3_4 and GPIO3_5 as board version 23.P18. Connect PCIE pin 39,41 to 3.3V 24.P18. Add DCDC for WiFi card CUS239,CUS260 PA 25.P8. Disconnect IRQ4 to VR500, connect IRQ4 to PCIE wake 26.P20.DNP L22 to disconnect 1V5 to PCIE 27.P23.delete R12,R18 28.P8.delete J15,set JTAG power to 3.3V 29.Change the board part number to X-T1023RDB-PC 30.P18, replace PCIe slot with low height connector , 1.6mm stand off 31.Replace the current sense IC 32.Add jumper to turn on/off DCDC for PoE test 33.P6 Delete C448 34.Add 2.5G port PoE support 35.P6 connect IFC_A21 to R315 directly for DDR4 type 36.P16 change R280 pull high to 1.2V 37.P13 add I2C expander for bank selecting 38.P6, add pull height resister to A25 and A26, delete A26 test point 39.P18, add DCDC for each card PA	C1

X-T1023RDB-PC

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Drawn by: Shanghai Team	Page Title: COVER PAGE		
Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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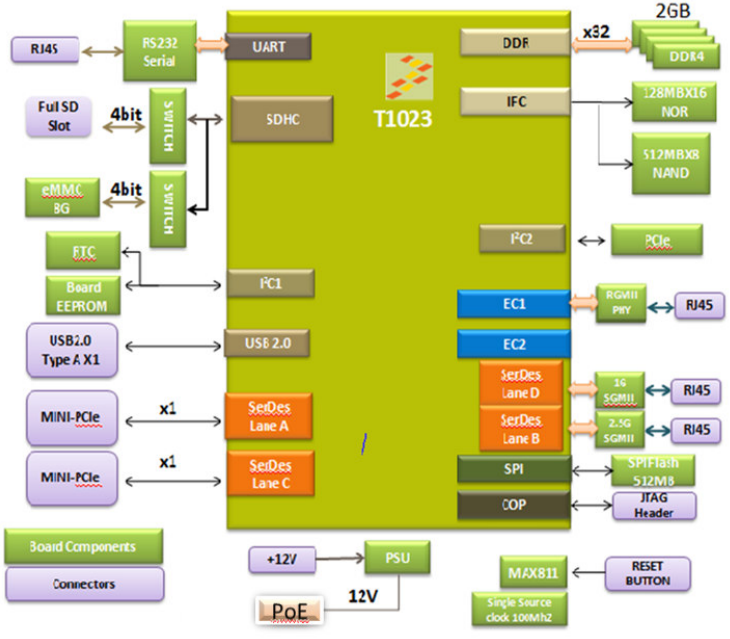
SYSTEM BLOCK DIAGRAM



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Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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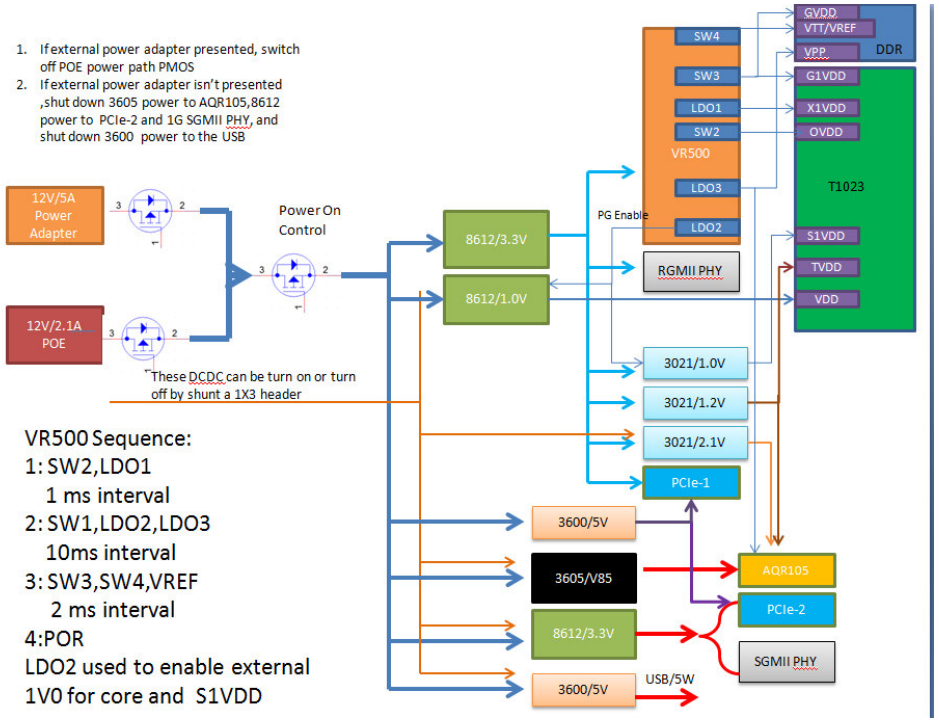
1. If external power adapter presented, switch off POE power path PMOS
2. If external power adapter isn't presented ,shut down 3605 power to AQR105,8612 power to PCIe-2 and 1G SGMII PHY, and shut down 3600 power to the USB



VR500 Sequence:
1: SW2,LDO1
1 ms interval
2: SW1,LDO2,LDO3
10ms interval
3: SW3,SW4,VREF
2 ms interval
4:POR
LDO2 used to enable external 1V0 for core and S1VDD

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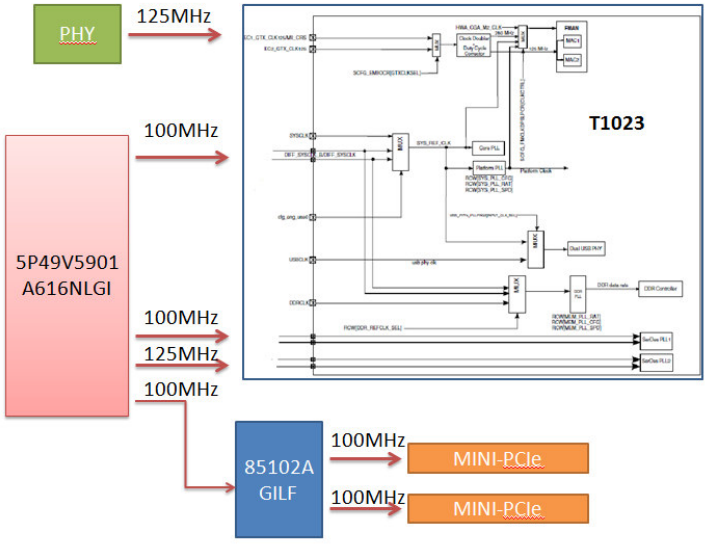
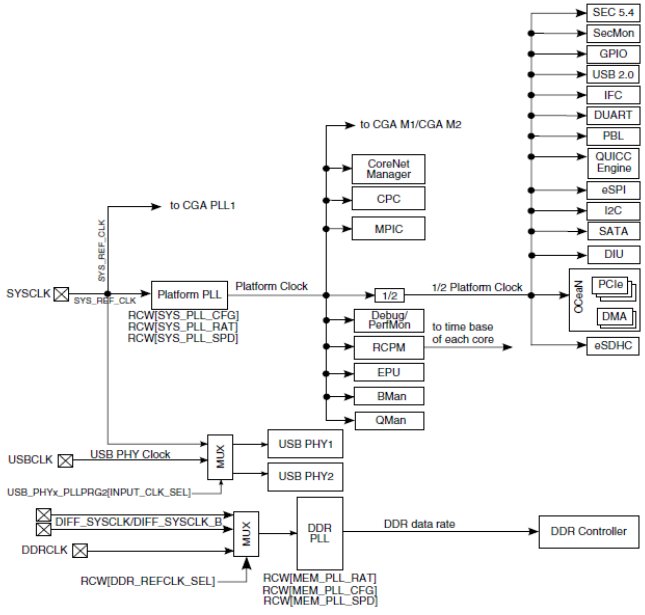
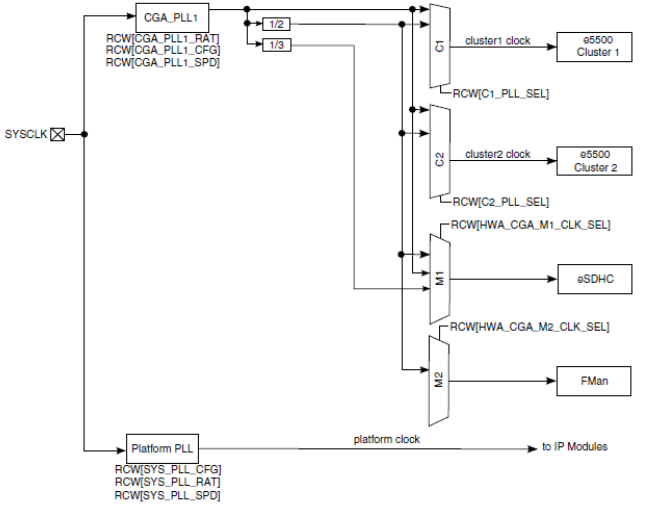
Single Clock Source







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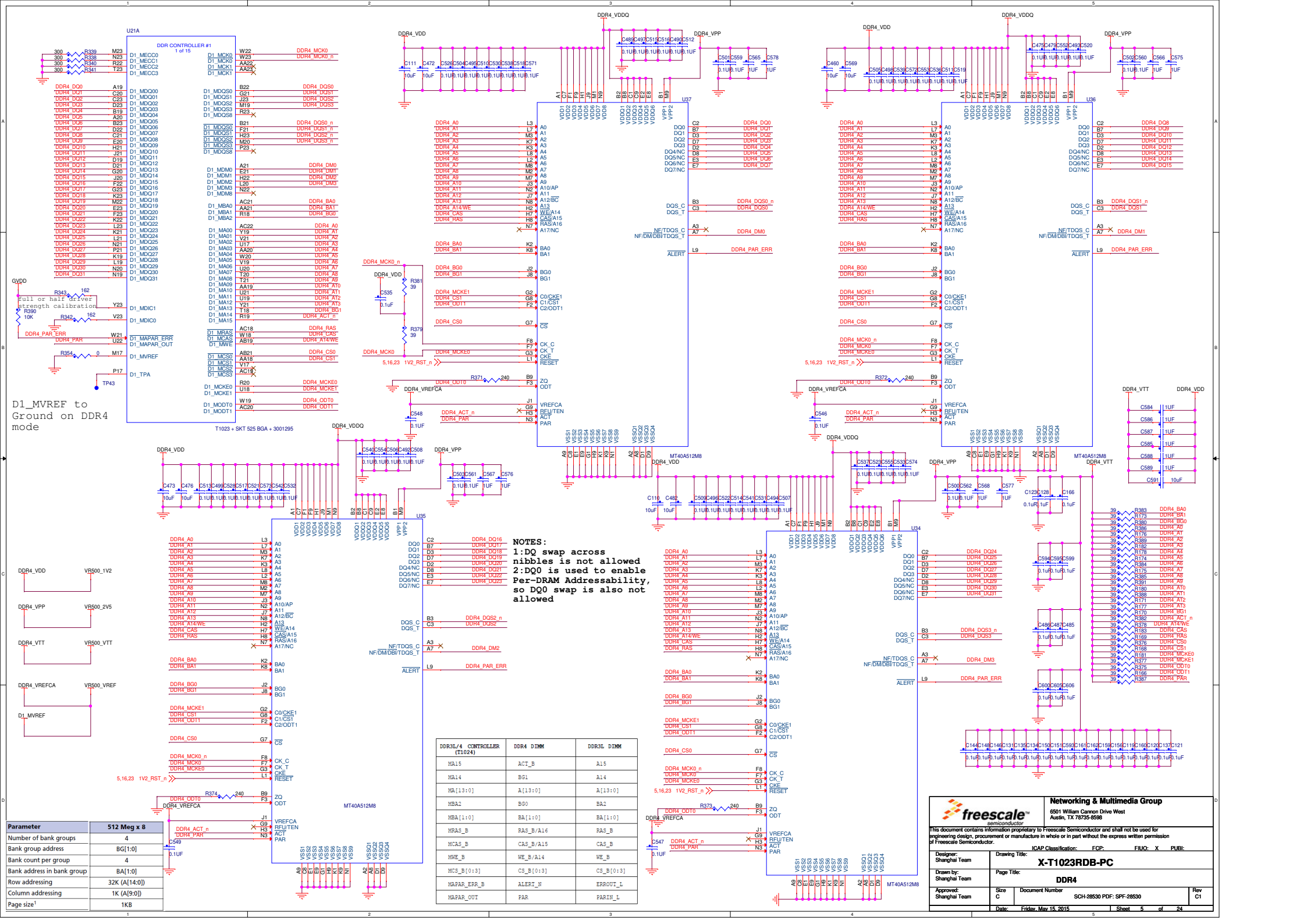

DDR3L/4 CONTROLLER (T1024)	DDR4 DIMM	DDR3L DIMM
MA15	ACT_B	A15
MA14	BG1	A14
MA[13:0]	A[13:0]	A[13:0]
MBA2	BG0	BA2
MBA[1:0]	BA[1:0]	BA[1:0]
MRAS_B	RAS_B/A16	RAS_B
MCAS_B	CAS_B/A15	CAS_B
MWE_B	WE_B/A14	WE_B
MCS_B[0:3]	CS_B[0:3]	CS_B[0:3]
MAPAR_ERR_B	ALERT_N	ERROUT_L
MAPAR_OUT	PAR	PARIN_L

Parameter	512 Meg x 8
Number of bank groups	4
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	32K (A[14:0])
Column addressing	1K (A[9:0])
Page size[1]	1KB

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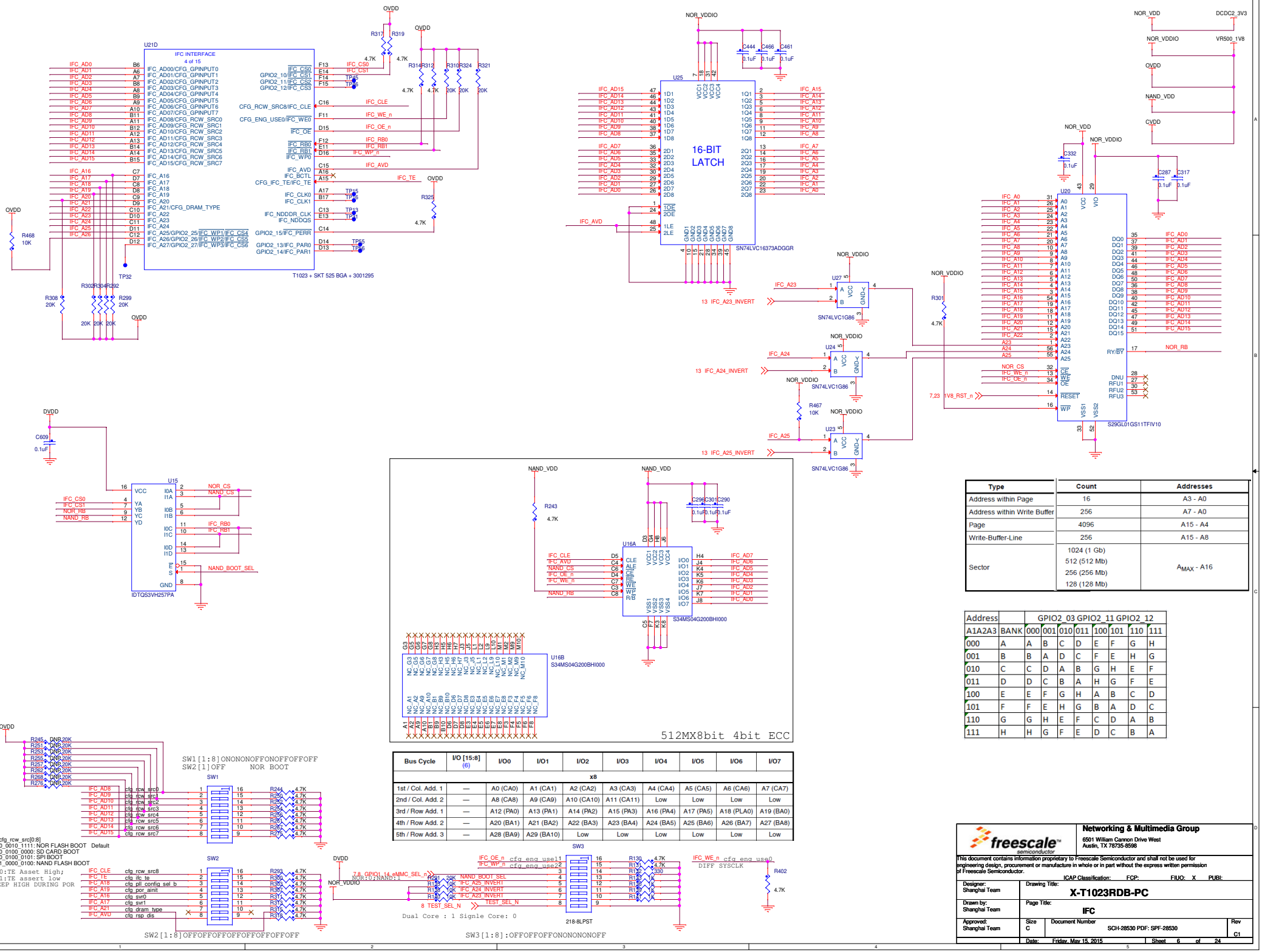

Type	Count	Addresses
Address within Page	16	A3 - A0
Address within Write Buffer	256	A7 - A0
Page	4096	A15 - A4
Write-Buffer-Line	256	A15 - A8
Sector	1024 (1 Gb) 512 (512 Mb) 256 (256 Mb) 128 (128 Mb)	A_{MAX} - A16

Address		GPIO2_03 GPIO2_11 GPIO2_12							
A1A2A3	BANK	000	001	010	011	100	101	110	111
000	A	A	B	C	D	E	F	G	H
001	B	B	A	D	C	F	E	H	G
010	C	C	D	A	B	G	H	E	F
011	D	D	C	B	A	H	G	F	E
100	E	E	F	G	H	A	B	C	D
101	F	F	E	H	G	B	A	D	C
110	G	G	H	E	F	C	D	A	B
111	H	H	G	F	E	D	C	B	A

Bus Cycle	I/O [15:8] (6)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st / Col. Add. 1	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd / Row Add. 1	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (PLA0)	A19 (BA0)
4th / Row Add. 2	—	A20 (BA1)	A21 (BA2)	A22 (BA3)	A23 (BA4)	A24 (BA5)	A25 (BA6)	A26 (BA7)	A27 (BA8)
5th / Row Add. 3	—	A28 (BA9)	A29 (BA10)	Low	Low	Low	Low	Low	Low

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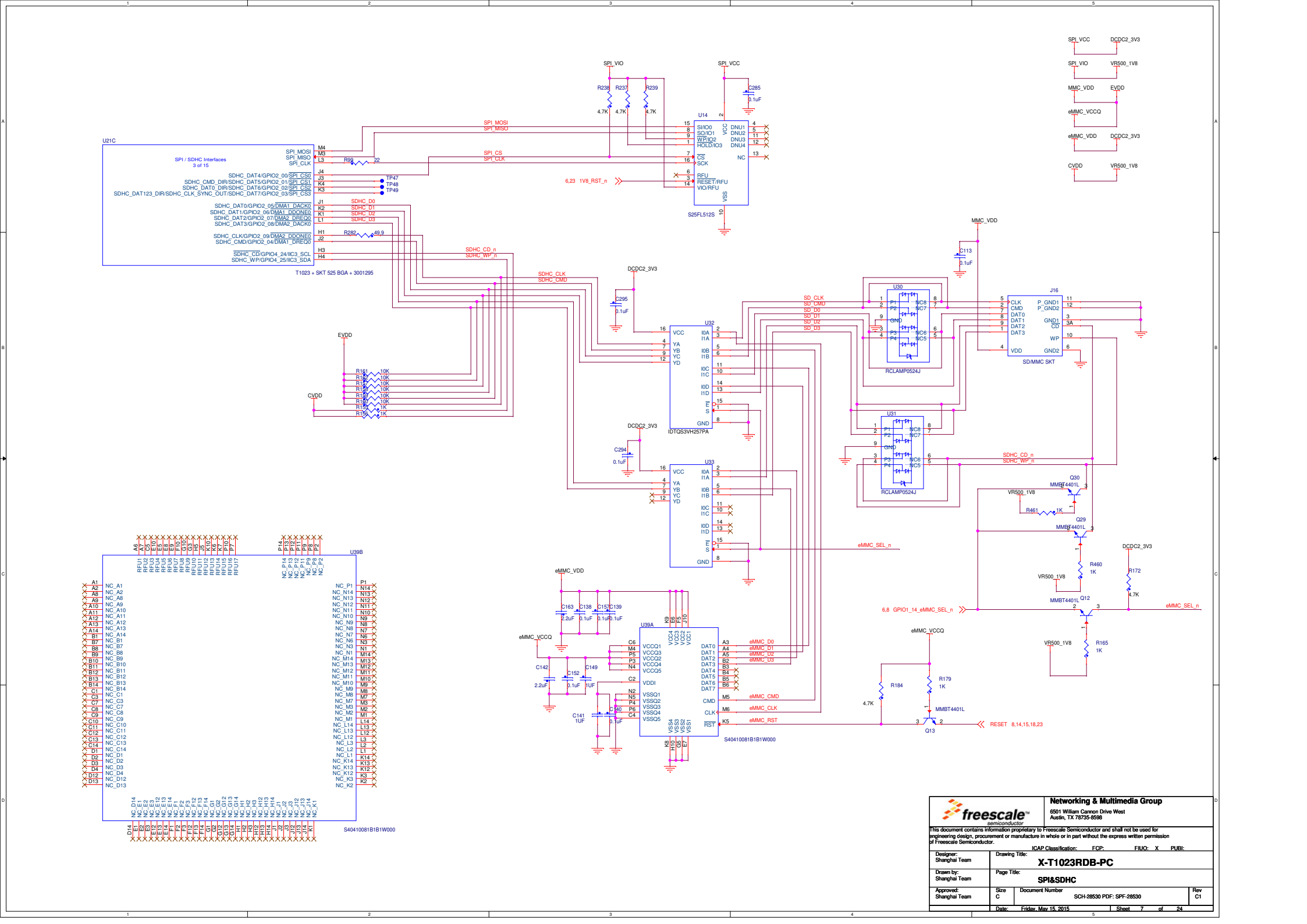

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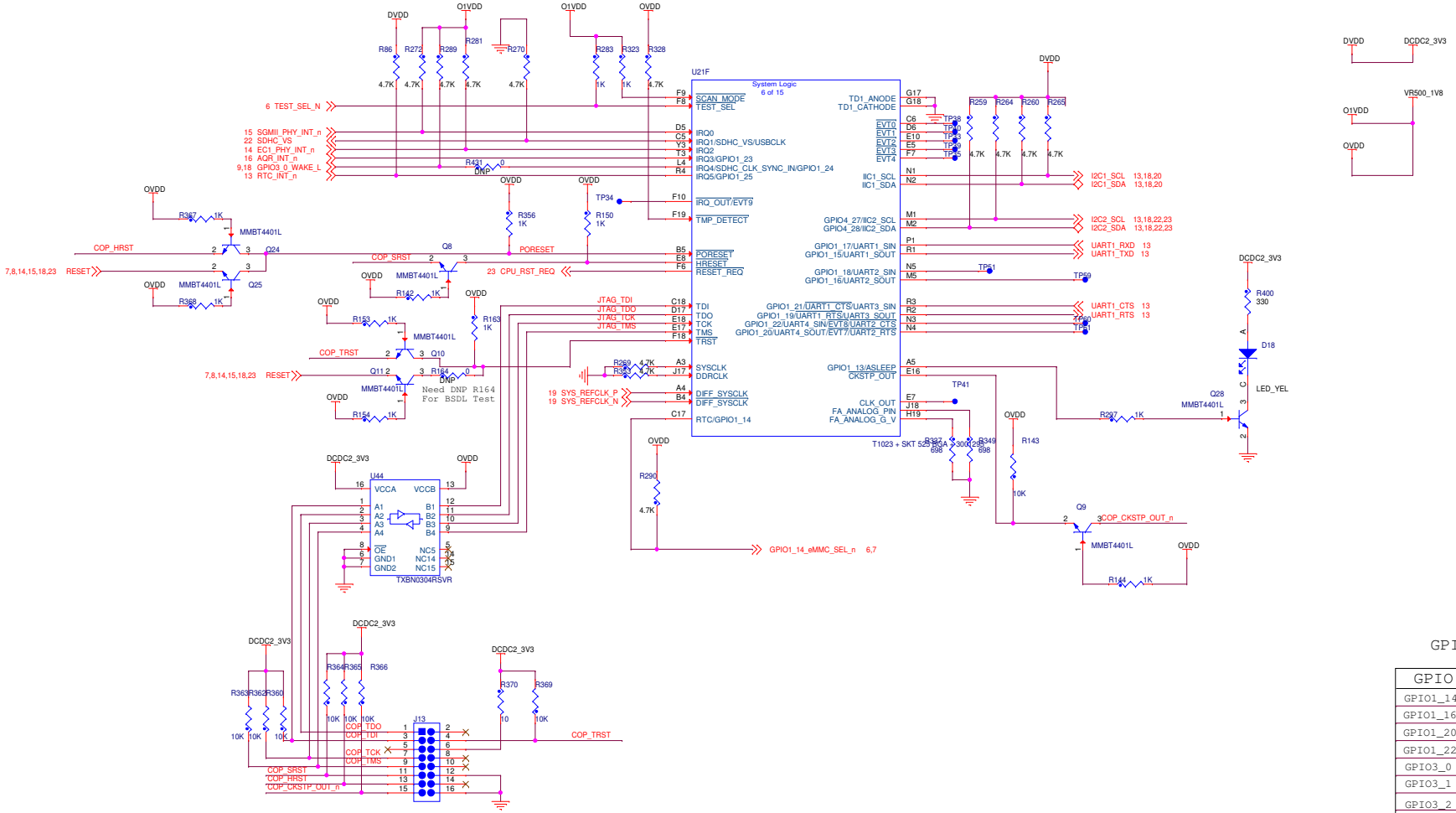

GPIO & INTTRUPT

GPIO	H	L
GPIO1_14	SD/MMC Card	eMMC
GPIO1_16		
GPIO1_20		
GPIO1_22		
GPIO3_0		PCIE1 wake
GPIO3_1		reserved
GPIO3_2		PCIE2 wake
GPIO3_3		reserved
GPIO3_4	Board version bit 1	
GPIO3_5	Board version bit 0	
IRQ0		1G SGMII PHY
IRQ2		RGMII PHY
IRQ3		2.5G SGMII PHY
IRQ4		PCIE1 wake
IRQ5		RTC

	Rev B	Rev D	Rev E	Rev F
GPIO3_04	0	0	1	1
GPIO3_05	0	1	0	1

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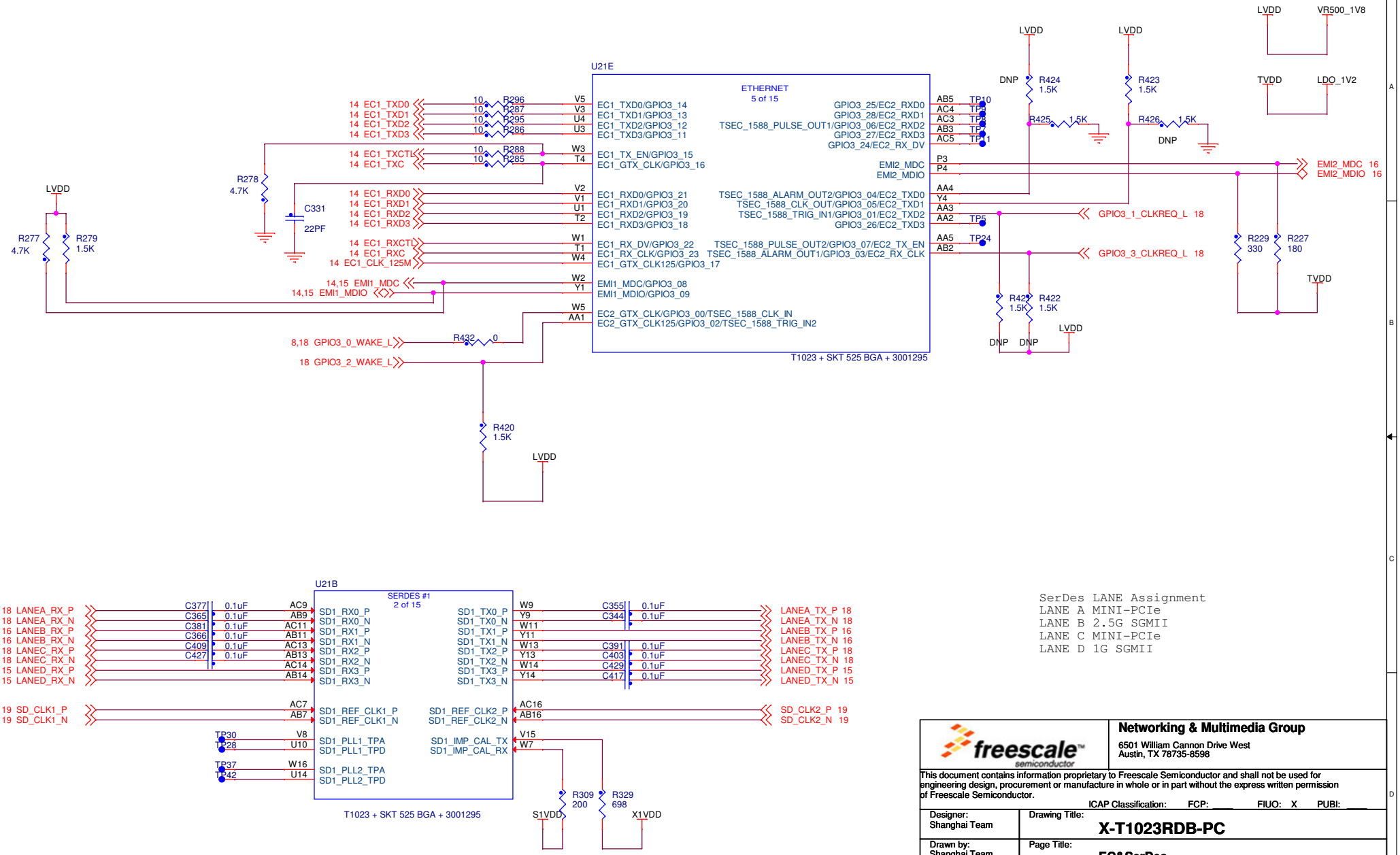

SerDes LANE Assignment
LANE A MINI-PCIe
LANE B 2.5G SGMII
LANE C MINI-PCIe
LANE D 1G SGMII

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Approved: Shanghai Team	Size B	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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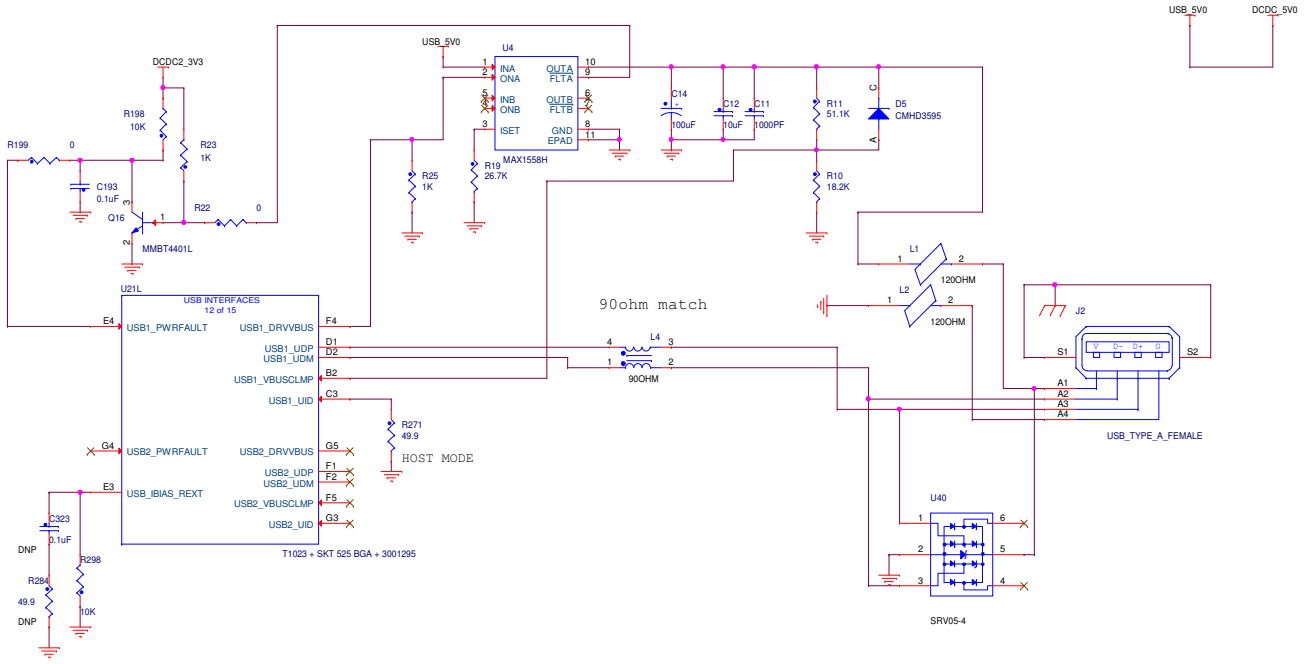

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Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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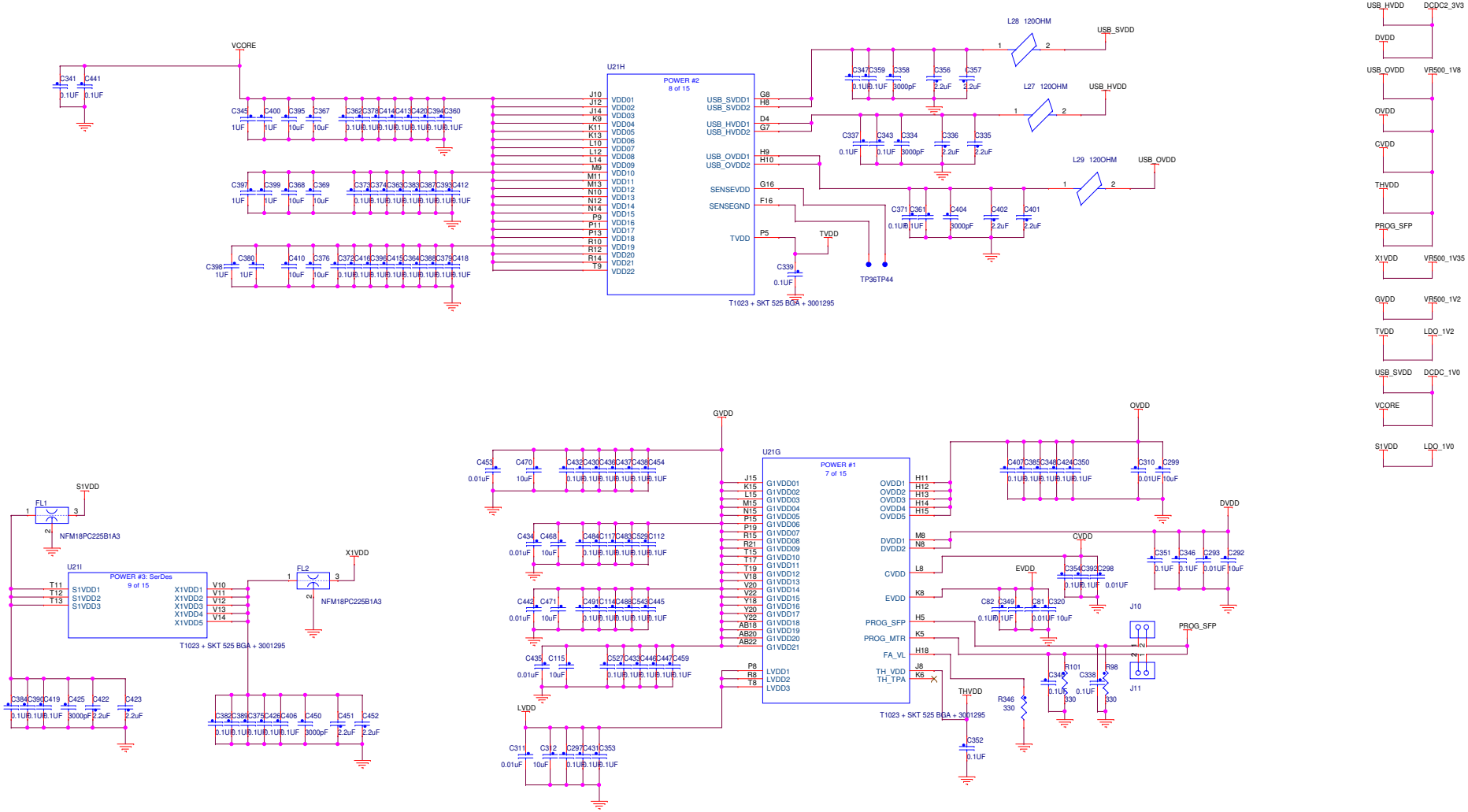

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Approved: Shanghai Team	Size: C	Document Number: SCH-28530 PDF: SPF-28530 Rev: C1
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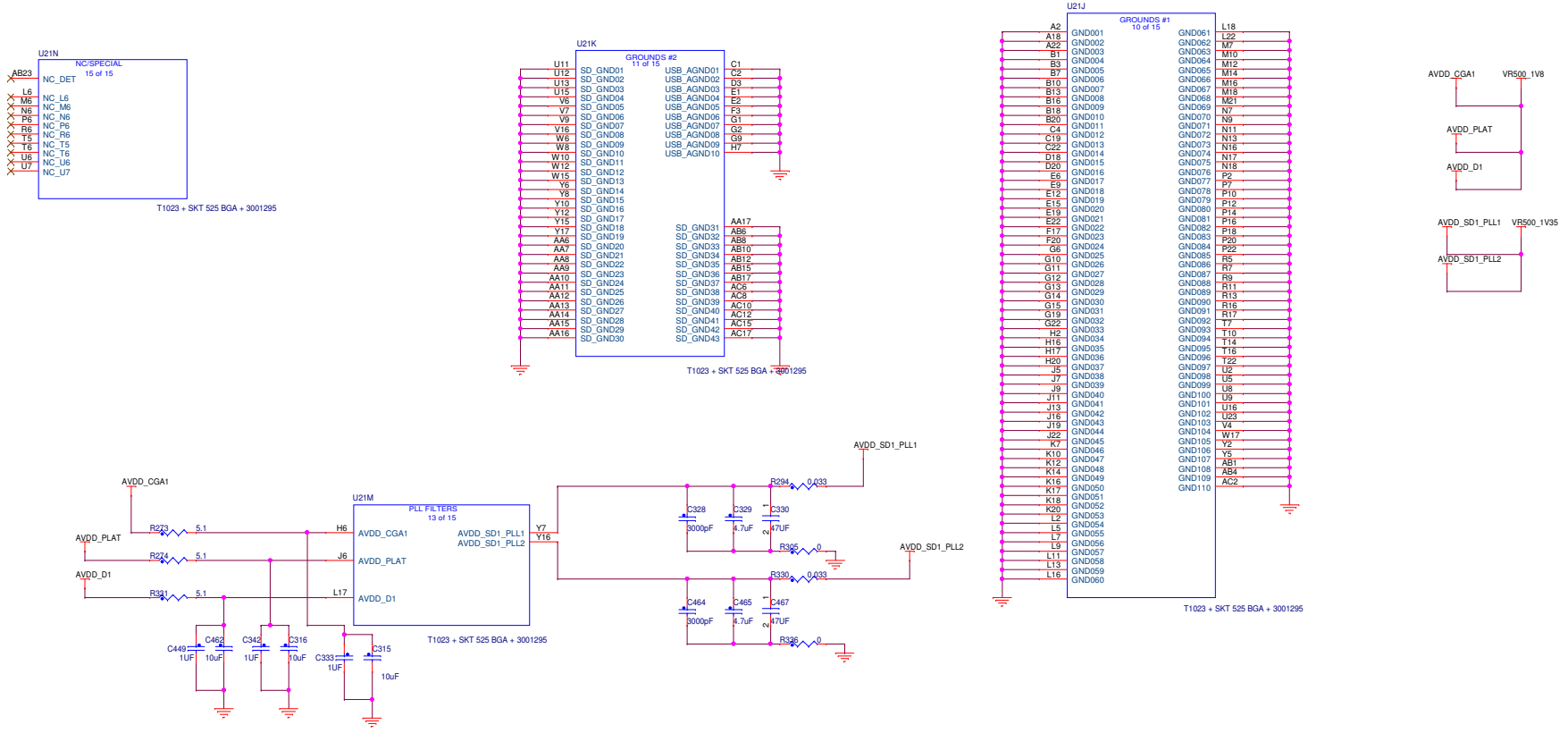

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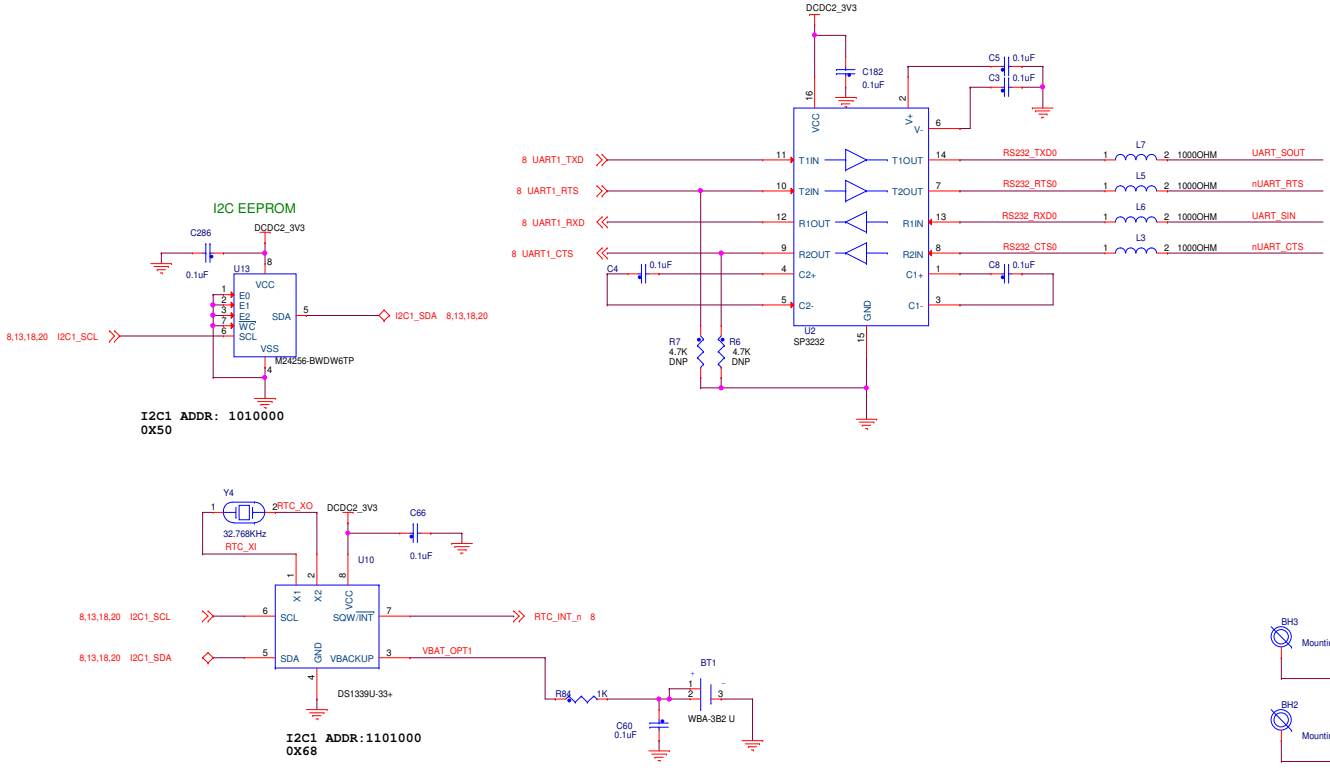

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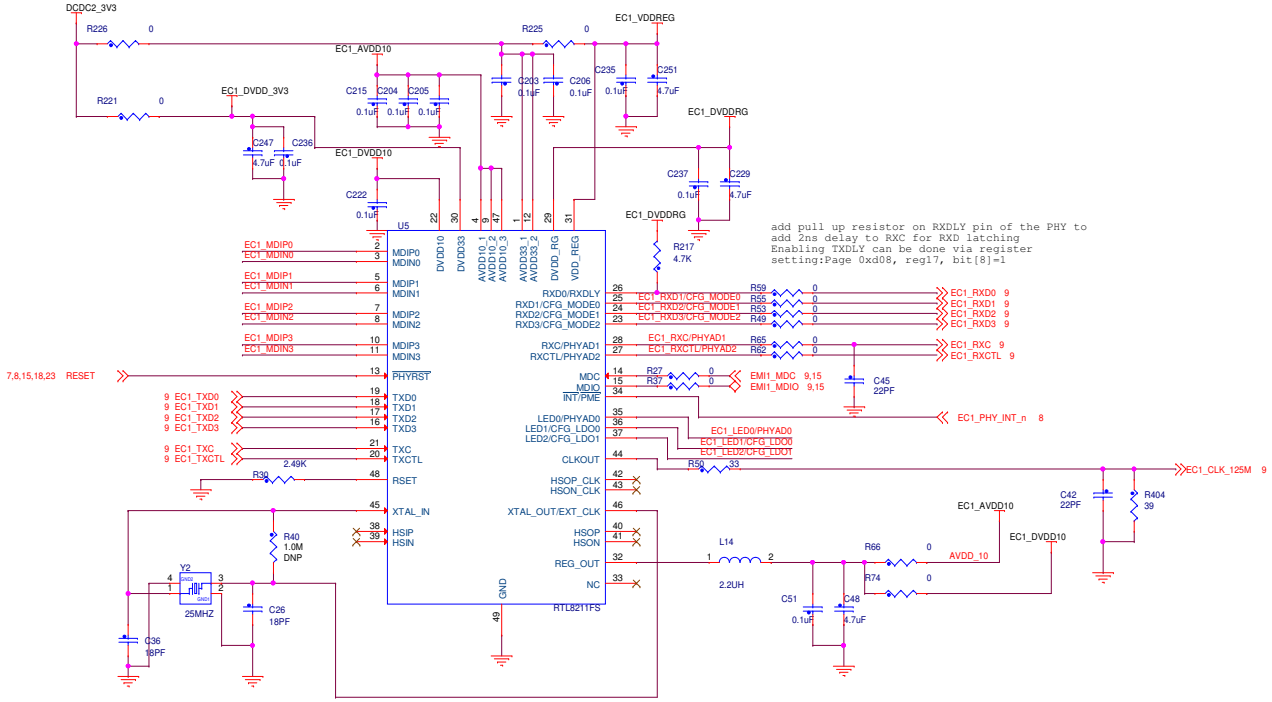
RGMII



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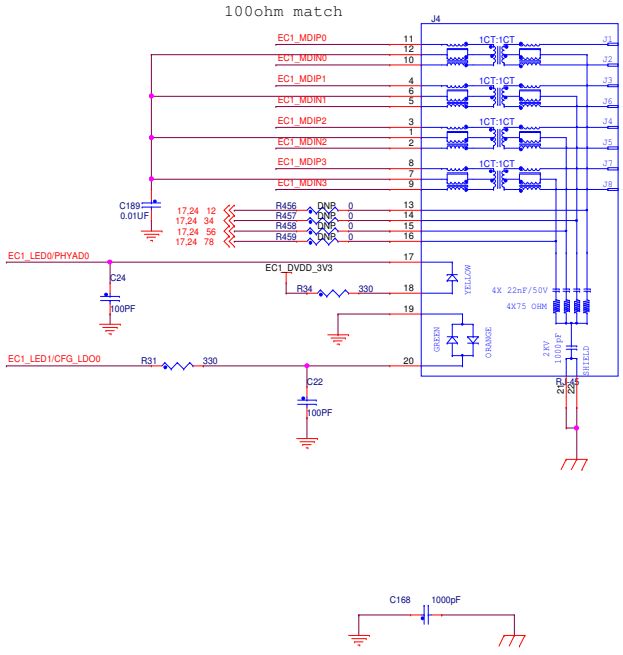


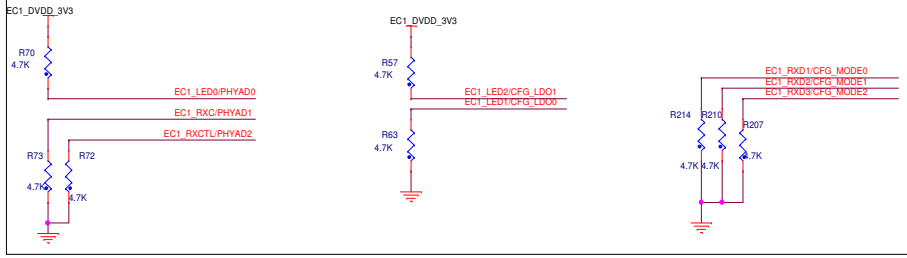
PHY CONFIGURATION:

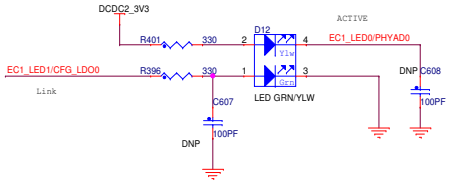
LED1(Green): LINK
LED0(Yellow): ACTIVE

PHY Address PHYAD[2:0]
1 3'b001

RGMII Power Source CFG_LDO[1:0]
External 3.3V 2'b00
Internal 2.5V 2'b01
Internal 1.8V 2'b10 (default)
Internal 1.5V 2'b11

UTP<<=>>RGMII
CFG_MODE[2:0] 3'b000





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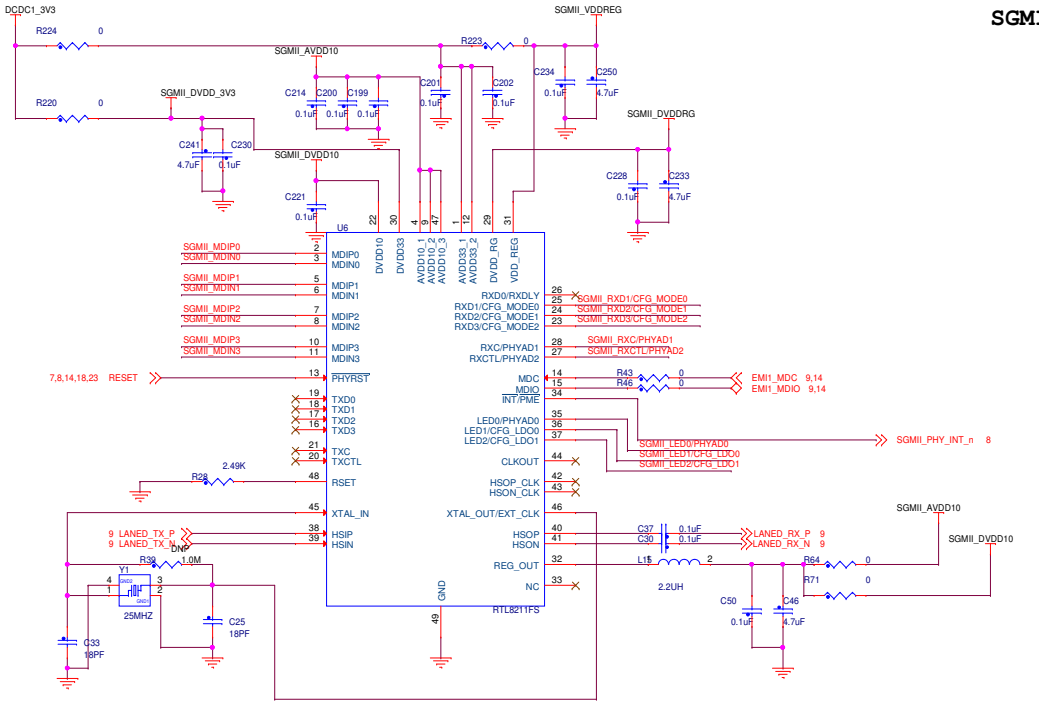
PHY 3V3 rise time should between 0.5ms~100ms
PHY internal LDO works after RESET deassert 50ms.

SGMII 1G



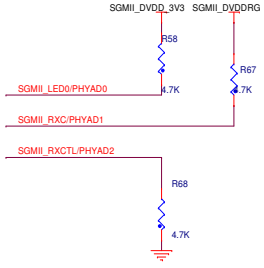
PHY CONFIGURATION:

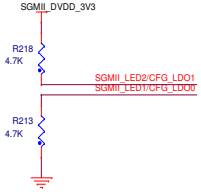
LED1(Green): LINK
LED0(Yellow): ACTIVE

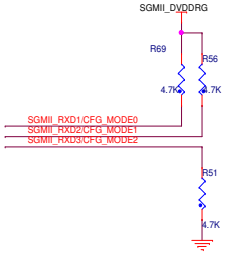
PHY Address PHYAD[2:0]
3 3'b011

RGMII Power Source CFG_LDO[1:0]
External 3.3V 2'b00
Internal 2.5V 2'b01
Internal 1.8V 2'b10 (default)
Internal 1.5V 2'b11

UTP<<=>>SGMII
CFG_MODE[2:0] 3'b011

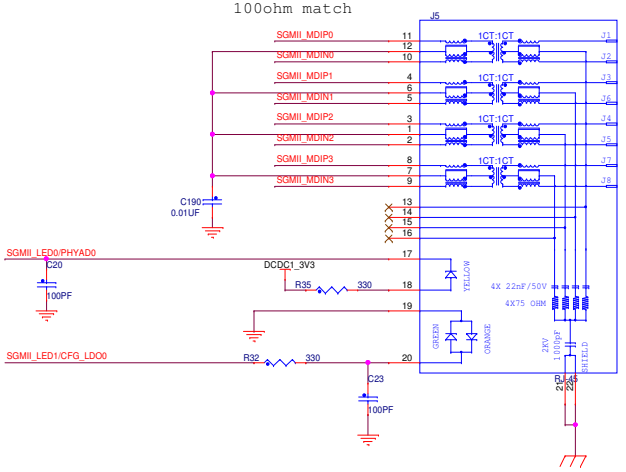


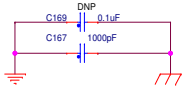


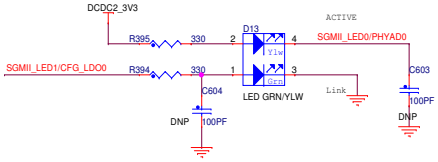


LABEL NAME:ETH2

100ohm match







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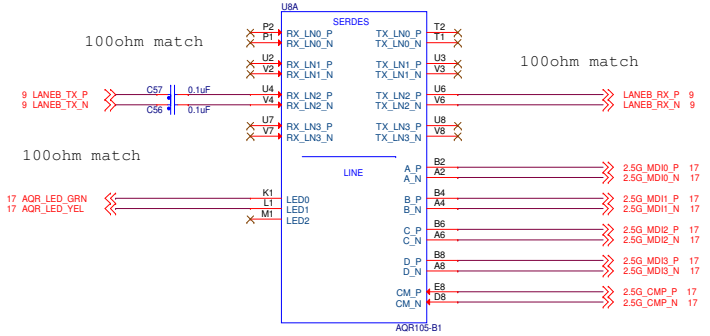
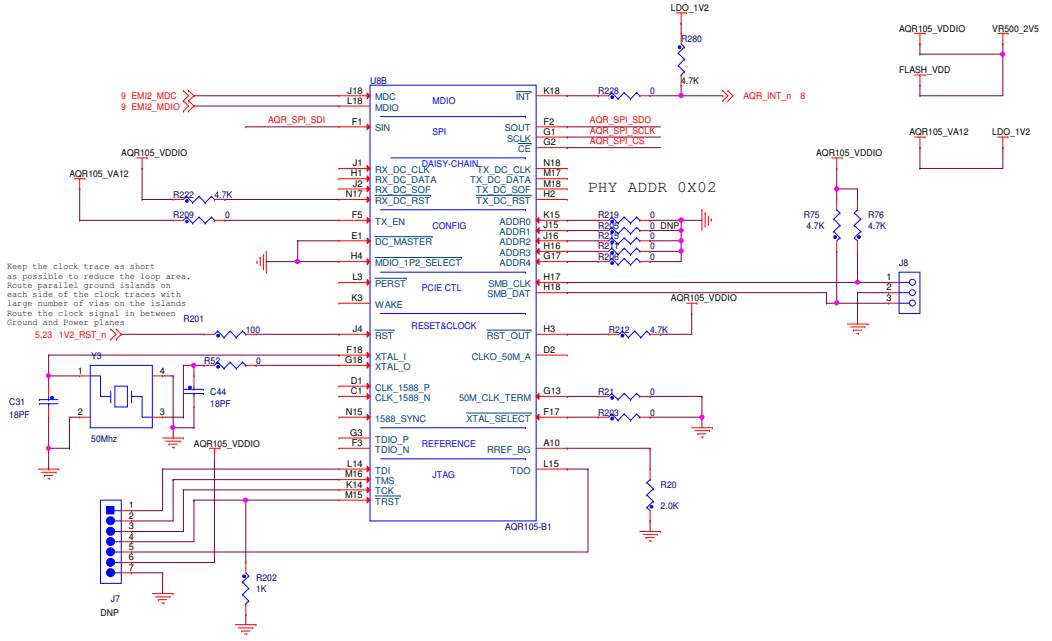
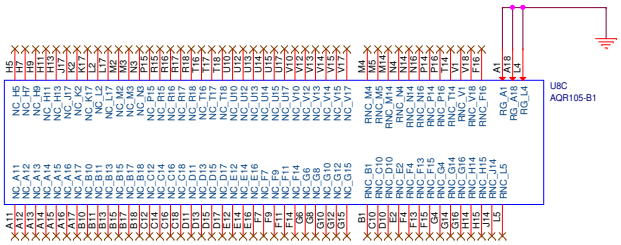
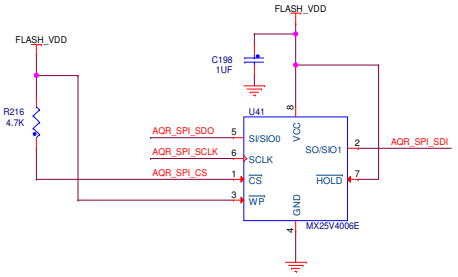




LANE 2 WORKS ON 2.5G SGMII MODE
PHY ADDRESS IS 0X02,EMI2
PHY INTERRUPT TO IRQ3





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Drawn by: Shanghai Team	Page Title: AQR105 2.5G		
Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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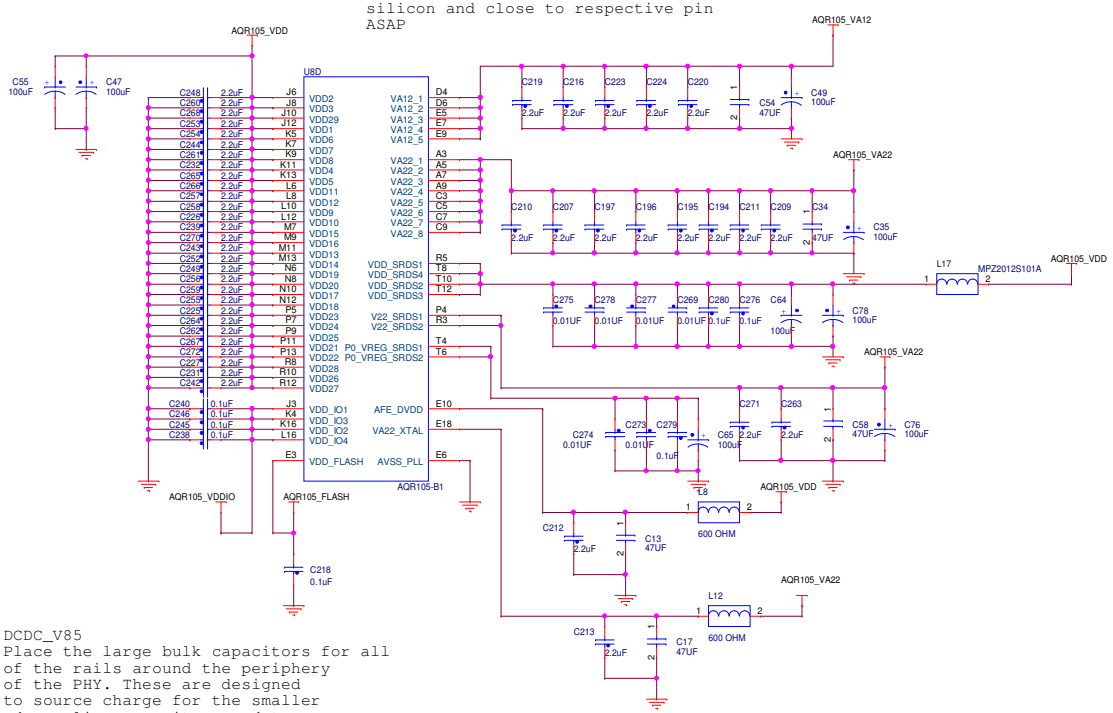
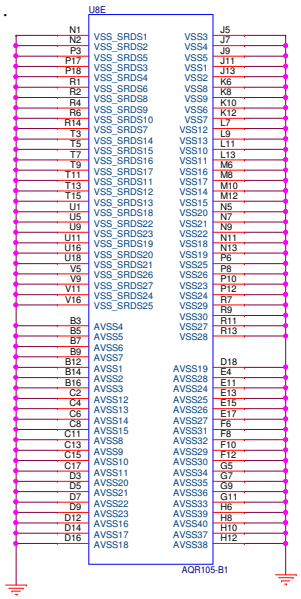
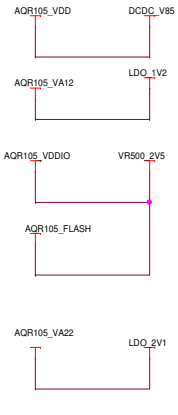
All the Caps should be placed under silicon and close to respective pin ASAP

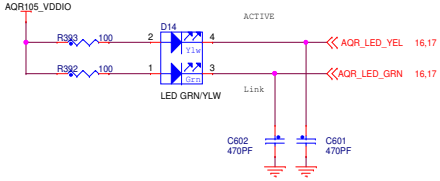


The 1.2V and 2.1V supplies are primarily analog supplies, and as such, all of the different analog power supply domains must be kept very quiet and separated via ferrite beads. These analog supplies must be kept away from the VDD and digital grounds to prevent capacitive coupling of noise into the analog circuitry. We recommend designing the PCB layer stack-up with ground shield planes above and below the analog supplies layer. The 2.1V rail for the 28nm PHYs requires a clean supply to ensure systems pass FCC

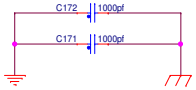




DCDC_V85
Place the large bulk capacitors for all of the rails around the periphery of the PHY. These are designed to source charge for the smaller decoupling capacitors and to smooth out ripple from the buck conversion process in the power regulators.
Run the VDD rail and Ground on internal planes
Use via-in-pad technology to maximize available area for decoupling capacitance.
Use epoxy-filled vias to prevent wicking during the reflow process
Use 15 mils traces and 12 mils vias for the power supply breakouts.

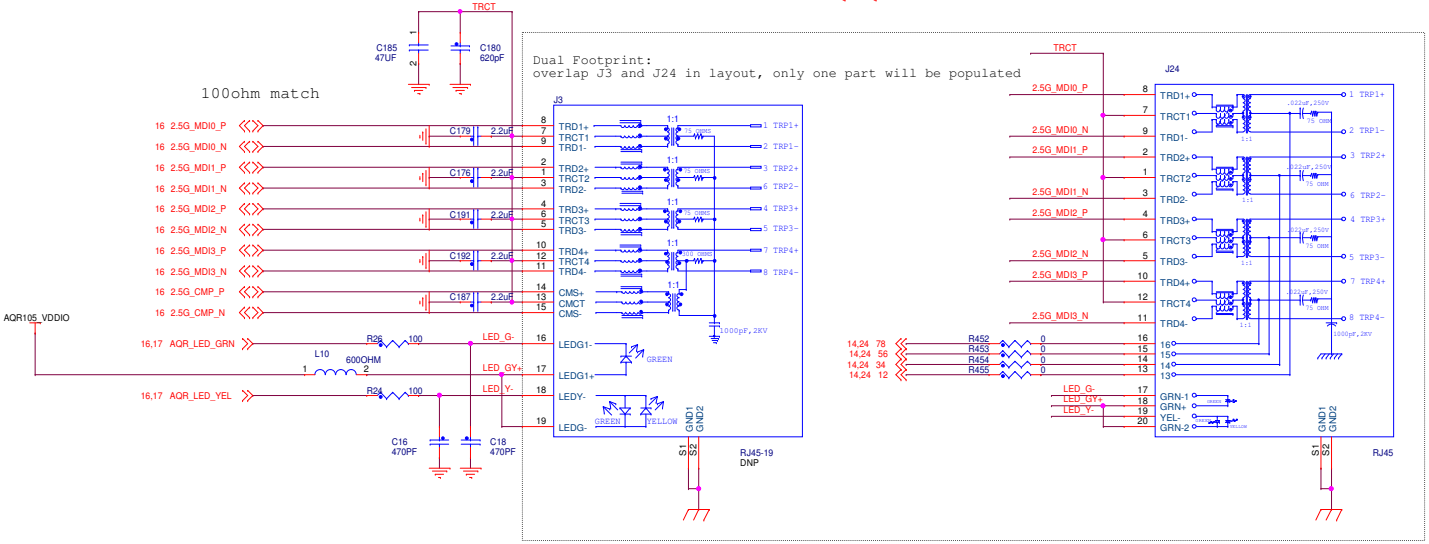


When routing LED signals to the cable connector or front panel, avoid running the traces too close in parallel with the XFI or BASE-T MDI signals on the same or adjacent layer. The separation must be at least 10x of the MDI signal trace width. If the LED signals need to run near the MDI traces, rout them on another layer that is separated by at least one power or ground layer



100ohm match

Dual Footprint:
overlap J3 and J24 in layout, only one part will be populated



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Drawn by: Shanghai Team	Page Title: AQR105 POWER		
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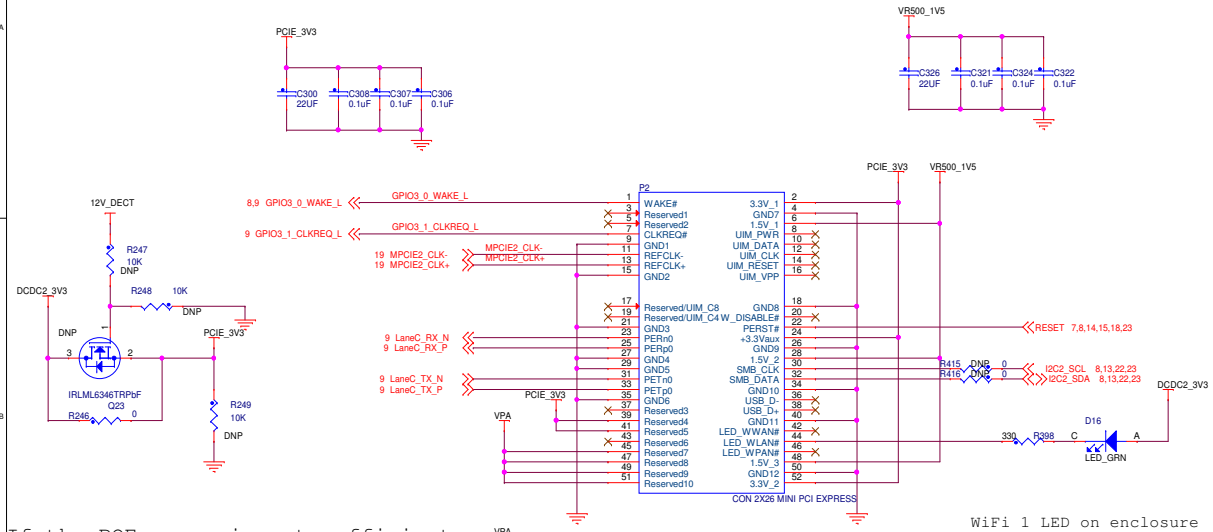
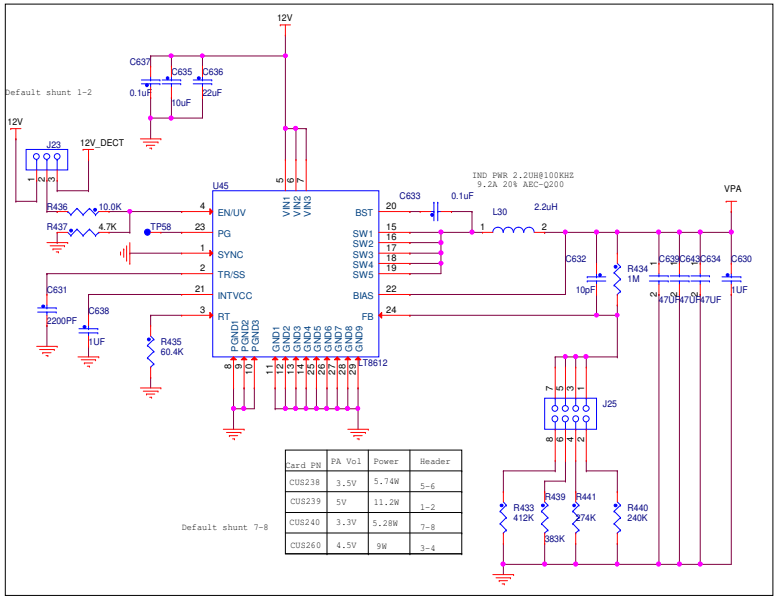
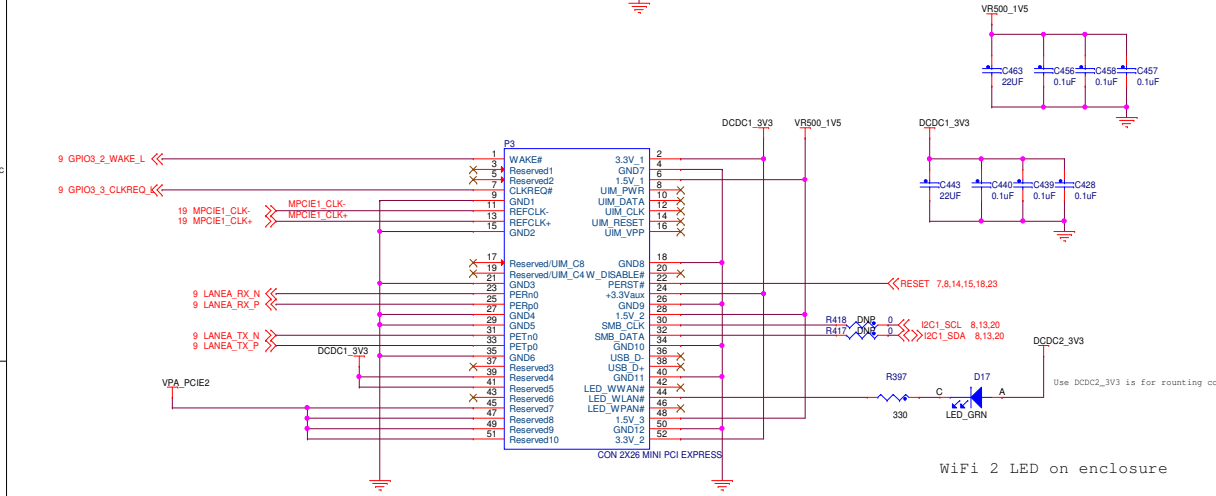
MINI-PCIe 1
WiFi 1 LED on Enclosure



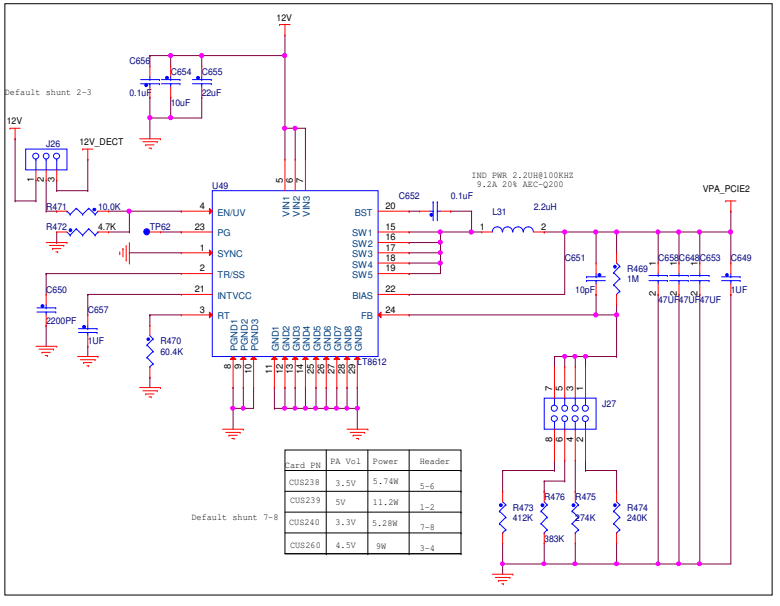


If the POE power is not sufficient DNP R291 and mount Q23 to shut down one PCIE power

WiFi 1 LED on enclosure



WiFi 2 LED on enclosure



MINI-PCIe 2
If only one card, should be inserted on PCIe 2 slot

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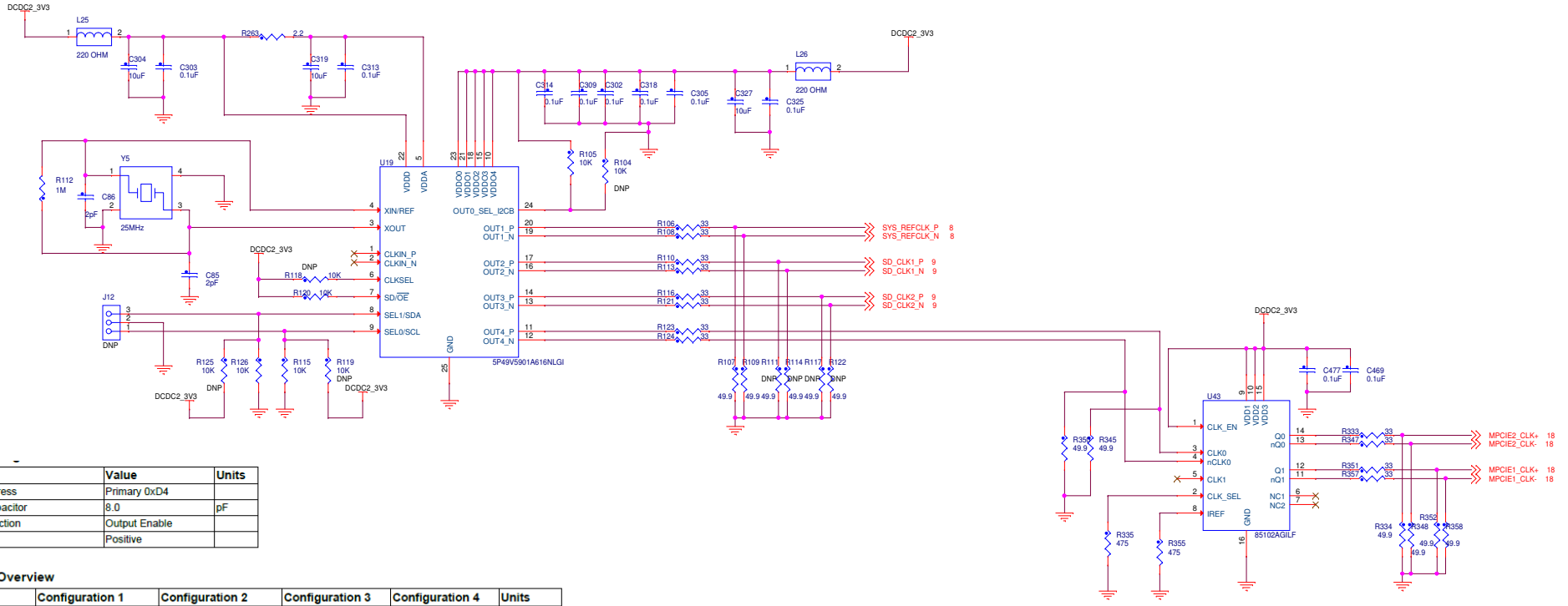
Drawn by: Shanghai Team	Page Title: PCIe		
Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
	Date: Friday, May 15, 2015	Sheet 18 of 24	



Parameter	Value	Units
Device I²C Address	Primary 0xD4	
XTAL Load Capacitor	8.0	pF
SD/OE Pin Function	Output Enable	
SD/OE Polarity	Positive	

Frequency Overview

Parameter	Configuration 1	Configuration 2	Configuration 3	Configuration 4	Units
Input	25	25			MHz
Output 0	25	25			MHz
Output 1	100	100			MHz
Output 2	100	100			MHz
Output 3	125	125			MHz
Output 4	100	100			MHz

Configuration 1 Parameters: SEL[1:0] = 00

Parameter	Output 0	Output 1	Output 2	Output 3	Output 4	Units
Input Frequency	25	25	25	25	25	MHz
Default Output Status	On	On	On	On	On	
VDDO Voltage	3.3	3.3	3.3	3.3	3.3	V
Output Type		HCSL	HCSL	HCSL	HCSL	
Frequency	25	100	100	125	100	MHz
Spread Spectrum		Off	Off	Off	Off	
Spread Spectrum Modulation						%
Slew Rate						
Phase Shift		0	0	0	0	Degrees

Configuration 2 Parameters: SEL[1:0] = 01

Parameter	Output 0	Output 1	Output 2	Output 3	Output 4	Units
Input Frequency	25	25	25	25	25	MHz
Default Output Status	On	On	On	On	On	
VDDO Voltage	3.3	3.3	3.3	3.3	3.3	V
Output Type		LVDS	HCSL	HCSL	HCSL	
Frequency	25	100	100	125	100	MHz
Spread Spectrum		Off	Off	Off	Off	
Spread Spectrum Modulation						%
Slew Rate						
Phase Shift		0	0	0	0	Degrees

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Drawn by: Shanghai Team	Page Title: CLOCK		
Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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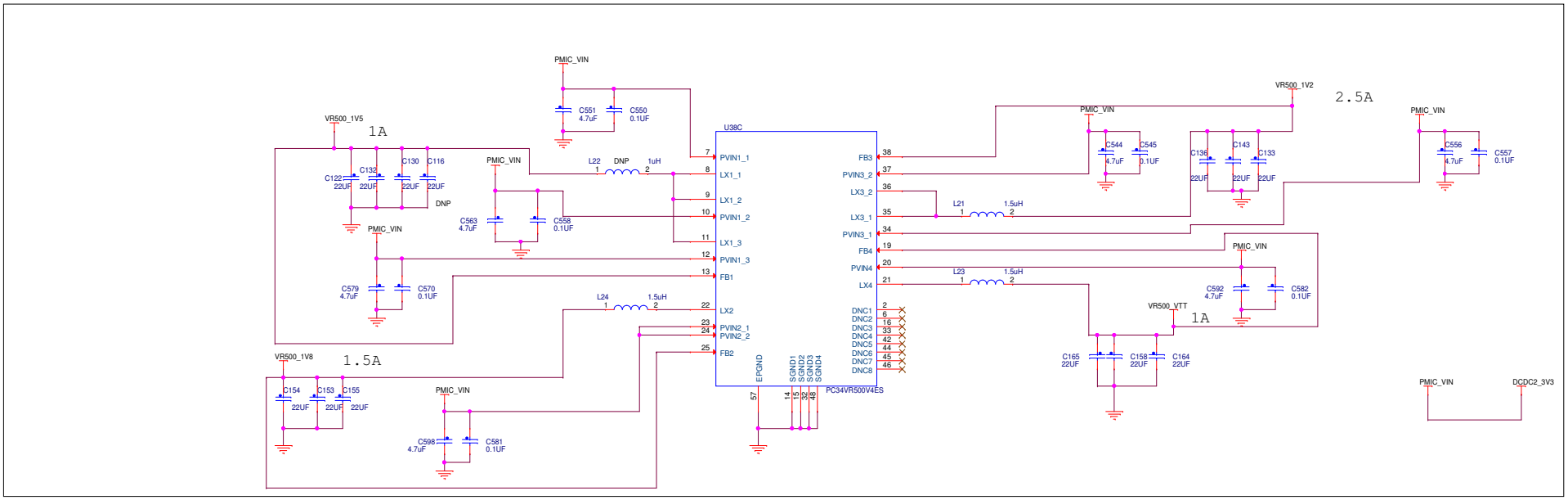

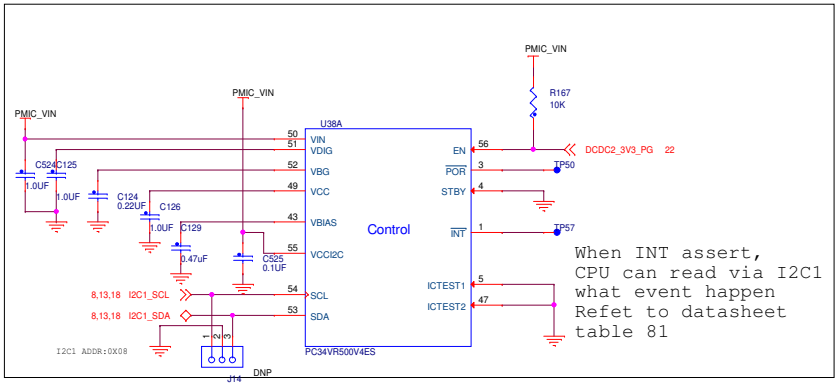

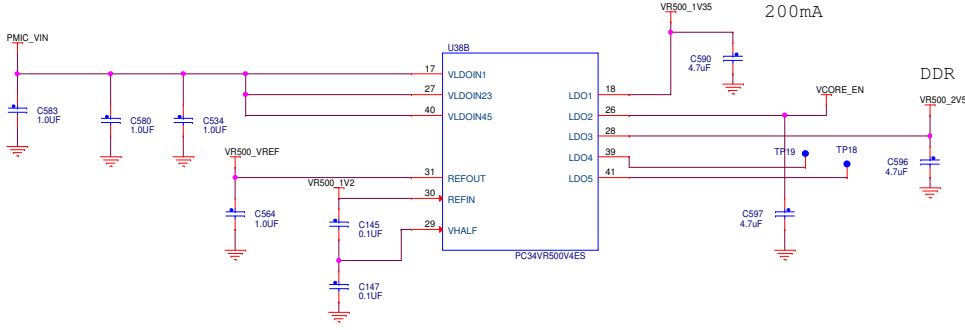

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Drawn by: Shanghai Team	Page Title: VR500		
Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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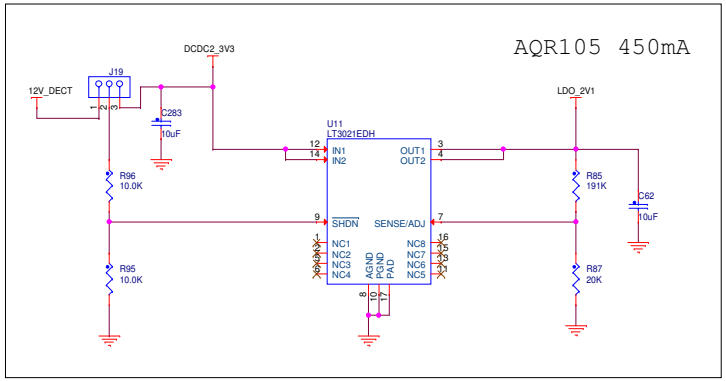
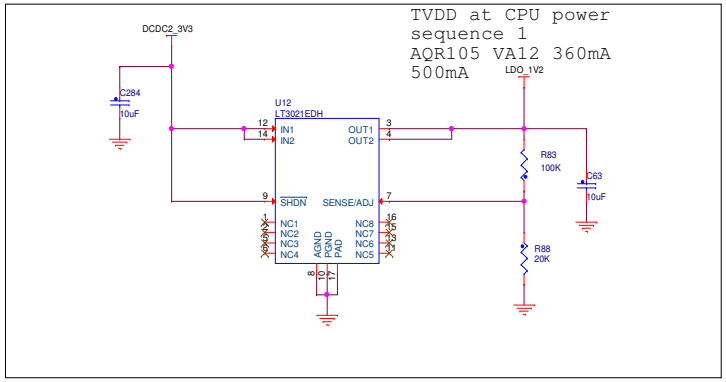
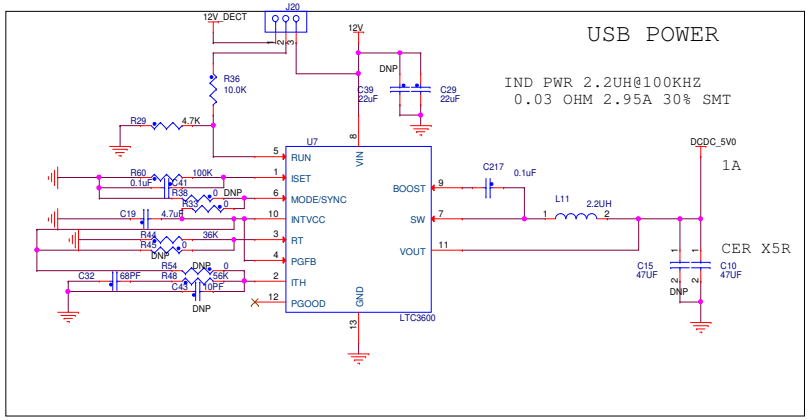
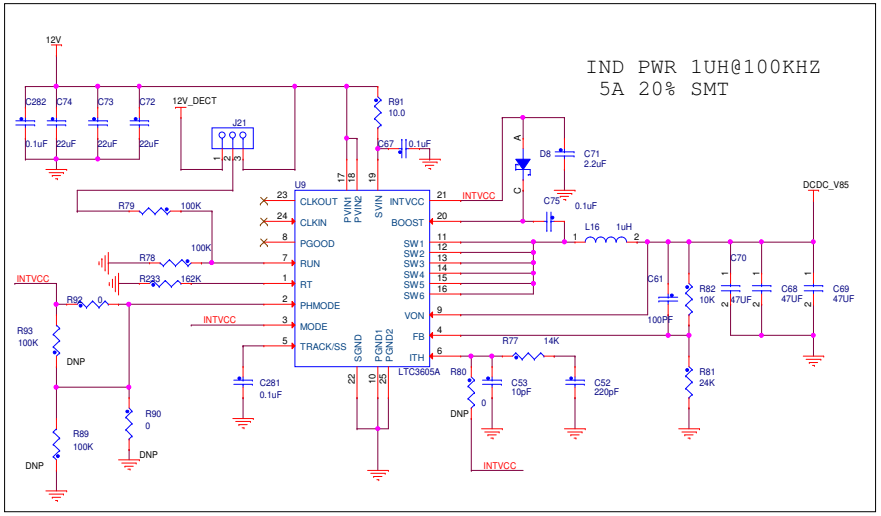
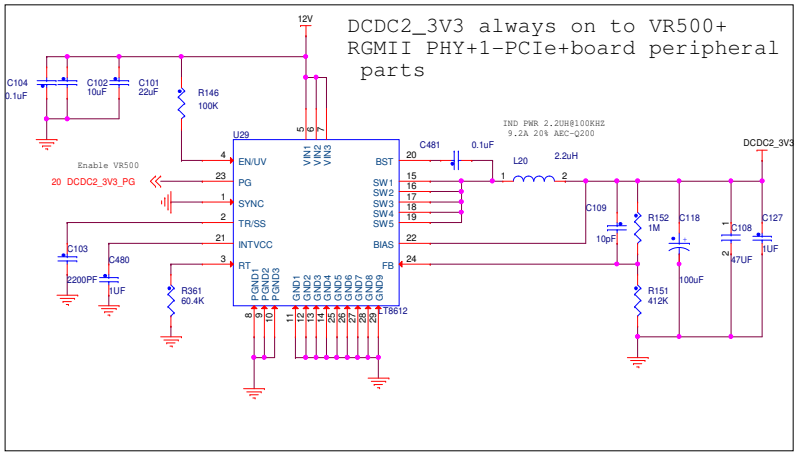


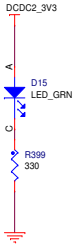




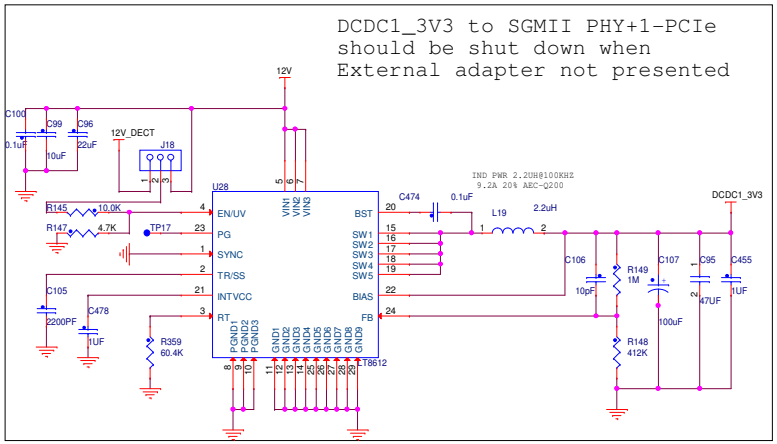


DCDC2_3V3 always on to VR500+ RGMII PHY+1-PCIe+board peripheral parts





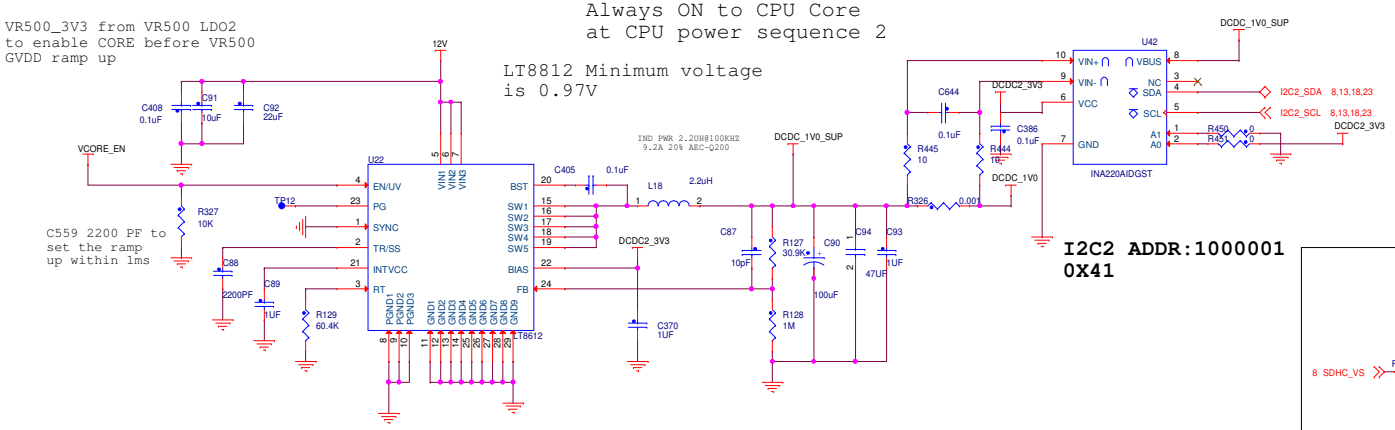
DCDC1_3V3 to SGMII PHY+1-PCIe should be shut down when External adapter not presented



VR500_3V3 from VR500 LDO2 to enable CORE before VR500 GVDD ramp up

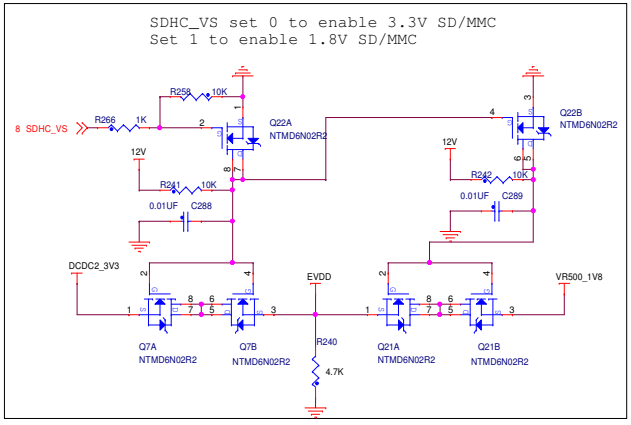
Always ON to CPU Core at CPU power sequence 2

LT8812 Minimum voltage is 0.97V

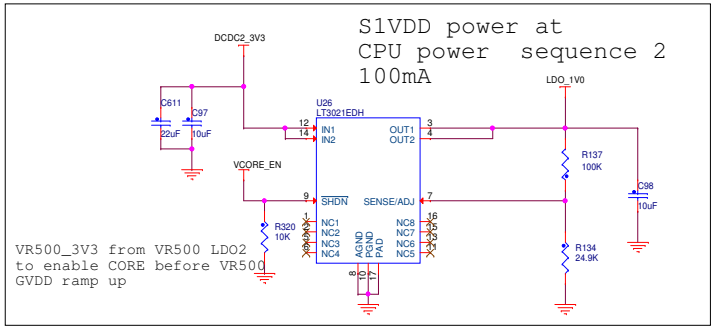


I2C2 ADDR:1000001 0X41

SDHC_VS set 0 to enable 3.3V SD/MMC
Set 1 to enable 1.8V SD/MMC



S1VDD power at CPU power sequence 2 100mA



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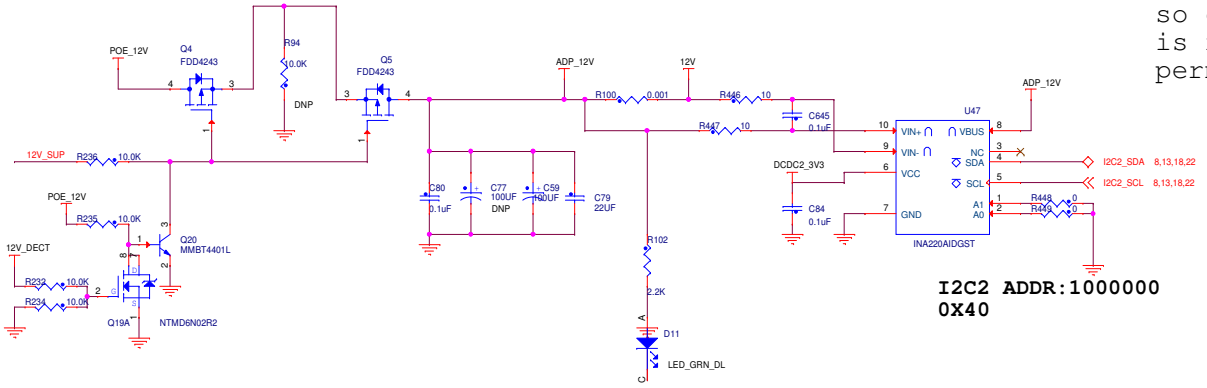
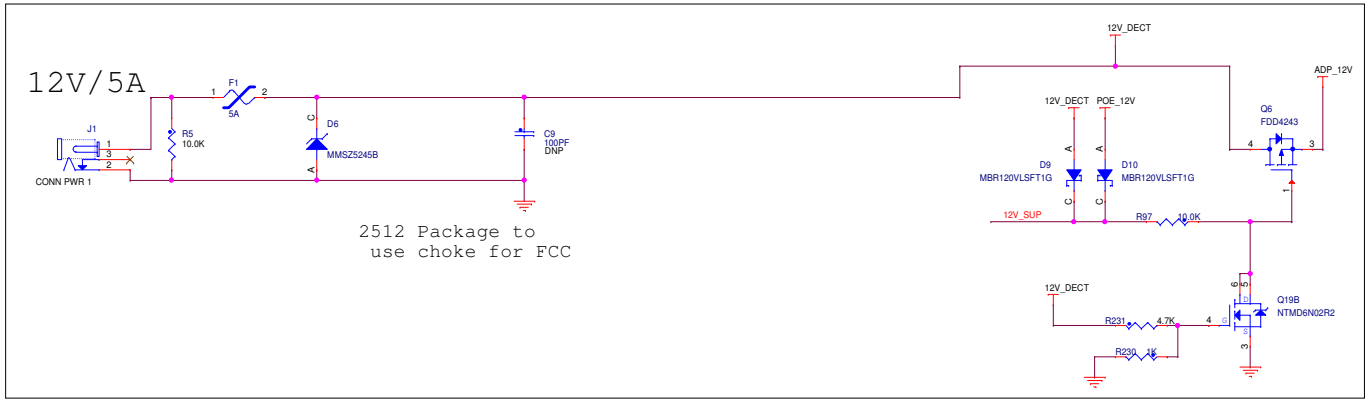
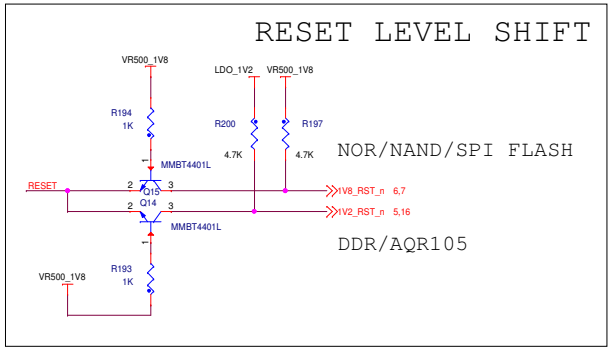
Casecade PMOS to prevent
adapter current flow backward
or POE current conduct through
body diode

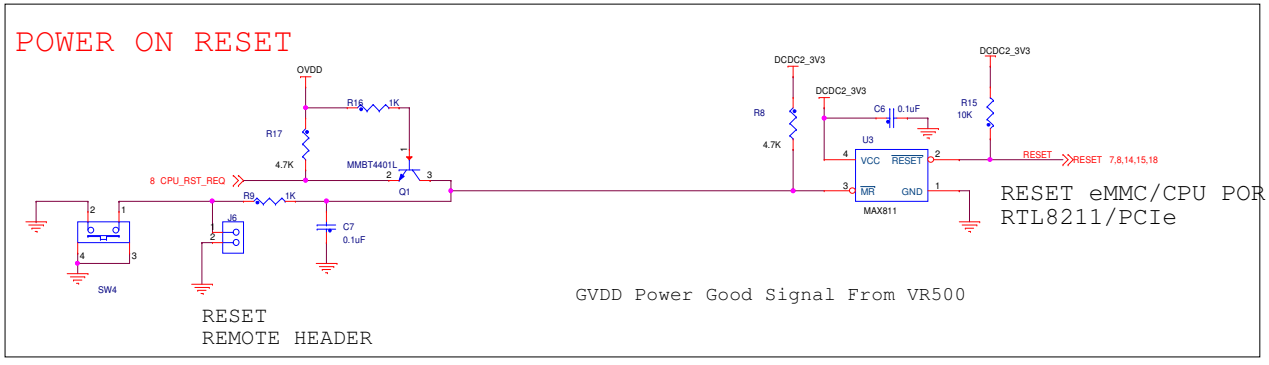
NOTES: External Power adapter
set higher priority than POE,
so only external power adapter
is not presented, then PMOS Q15 is
permited to conduct the POE power



I2C2 ADDR:1000000
0X40







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Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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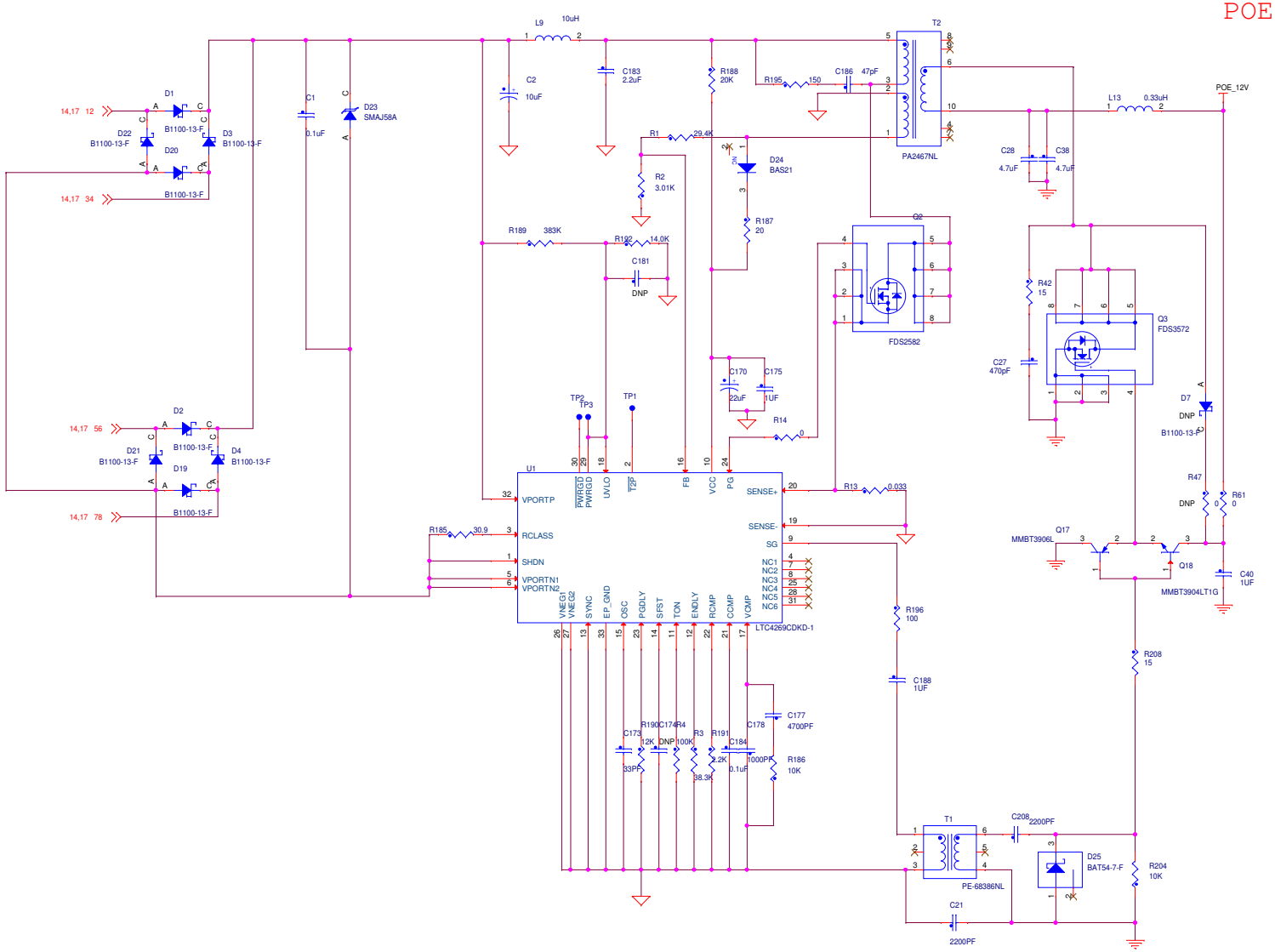
POE 12V/2.1A, 802.3.at



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Approved: Shanghai Team	Size C	Document Number SCH-28530 PDF: SPF-28530	Rev C1
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