Expanding the COM Express® Specification for Alternative Microprocessor Architectures

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1 Introduction

Since its introduction in 2005, the COM Express® form factor has shown increasing market acceptance within the industry landscape. Customers have been attracted to a number of features:

- Small size (125 mm x 95 mm)
- Low power
- Flexible I/O
- Design risk mitigation and time to market advantage since CPU, memory, core power, BIOS and OS/drivers are already designed and validated
- Reuse of carrier design over successive processor generations

These features allow vendors to focus on their strengths of generating hardware tailored to their application (via an application-specific carrier board design), as well as application-level software and system integration.

The COM Express specification is built largely upon the x86 personal computer (PC) architecture, which has been successfully used in products scaling from hand-held medical equipment, digital kiosks and gaming, to in-vehicle infotainment. However, developing compliant modules based on non-x86 architecture CPUs is not supported by the specification. Requirements for highly x86-specific interfaces preclude the development of compatible modules using processors built on Power Architecture®, MIPS® or ARM® technologies. These System on Chip (SoC) processor architectures also have products that are highly scalable across a wide range of markets and applications.

This paper discusses solutions to deal with these cross-architecture and cross-market needs without changing the physical structure of the COM Express form factor. Maintaining the physical aspects of the form factor is important to leverage existing investments while creating additional, more deeply embedded opportunities for the standard.

There is a desire to ensure continued compatibility with today's standard COM Express modules. Target compatibility would entail:

- Physically plugs into an existing COM Express carrier
- Installed module does not damage itself or the carrier (carriers designed to the Carrier Design Guide are required to keep power off if module type does not match what the carrier can support)
- Consideration for compatibility to a current definition (such as Type 1 definition for the AB connector), if possible, and possibly at a lesser functionality level
- Application-specific interfaces differentiated between module types via differing definition of the CD connector

Leveraging an existing type as a starting point would be a good approach to meeting these goals.

This paper does not suggest abandoning COM Express compliant modules, but serves to start discussion on non-x86 SoC implementations in a move toward even broader market adoption.

2 Addressing the design challenges

2.1 Pins that are not offered by the SoC processor

There are a number of primary signals that come to mind when first grappling with the notion of developing a non-x86 COM board:

- Low pin-count bus: x86-only successor to ISA, once used for firmware flash, generally used today for legacy SuperIOs and TPMs
- Speaker: no longer used for BIOS acknowledgement
- HD Audio: x86-only interface for providing audio (requires external CODEC)
- A20Gate and KBRST: x86-only signals for legacy keyboard control, required by some legacy BIOS
- PROCHOT# and THERMTRIP#: signals for notifying the system that the processor is exceeding internal thresholds
- SM bus: not typically found on non-x86 processors
- Low-power sleep state pins assigned for x86 processors

Embedded processors based on Power Architecture, MIPS and ARM technologies do not provide such signals. These signals are truly x86-only.

Additionally, there are several interfaces seen to a lesser extent on SoCs than on x86 devices:

- SPI: seen on some non-x86 devices, for interface to low-speed peripherals such communication ports, control of external low-speed modules and flash memory.
- USB: seen on many non-x86 devices, but not to the extent seen on PC-architecture. Usually two ports, versus the 10+ typically seen on x86 chips.
- Standby power rails: typically not seen on embedded SoC processors.

The COM Express specification allocates signals for a variety of video interfaces:

- LVDS
- VGA
- SDVO (x86only)
- TV-OUT

Many deeply embedded non-x86 applications require HMI-like interfaces, and therefore require the video signals found on the COM Express definition. This requires maintaining LVDS and VGA video signals in the definition.

2.2 Value-added functions provided by the SoC processor, but not part of the pin-out

Embedded SoC processors of the type being considered in this paper also often have interfaces that are not covered by the COM Express specification. These include:

- Local Bus for interface direct to flash memory and other peripherals
- Ethernet MACs with RGMII, SGMII or XAUI interfaces
- Serial RapidIO® or other SerDes interfaces
- Multiple UART and I²C interfaces
- Industry-targeted interfaces like CANbus, TDM and non-Ethernet industrial communication protocols

Such interfaces should be considered to open up new application and market classes for the COM Express specification. These market opportunities include, but are not limited to, industrial control, IP telephony, networking and communications.

Note that one will see similar challenges even when considering the x86-based Intel® EP80579 SoC in a COM Express design. So while this paper directs attention to non-x86 interfaces in the section above, an SoC-oriented definition could conceptually help enable x86 SoC-based solutions as well.

Potential solutions to this challenge:

1. Redefine pins used by the specification for other purposes. This has challenges in itself:
   - There must be available pins to do this
   - Pins must be defined as benign when used in a compliant carrier
   - Pins will provide additional function when plugged into a compatible carrier
2. Standardization: as additional bus types are needed, the COM Express standard has evolved to create new types of modules, supporting the latest I/O requirements.

An example for a potential resolution for 1 and 2 above is to add a very SoC-specific interface like a TDM bus for IP telephony usage. This is a new interface that may not fit on the precious remaining reserved pins, and likely requires replacing older legacy interfaces like the Type2 PCI or IDE bus.

2.3 Firmware differences

Firmware for x86 processors typically provides plug and play enumeration of devices, which works well for detection and configuration of devices on the carrier in COM Express usage. A keyboard and mouse may be supported by USB, and a variety of boot media options are supported natively.

Contrast this with typical non-x86 processor bootup: devices may have hard-coded addresses and not enumerated–carrier PCI Express® devices and USB hubs will require enumeration at firmware time to be used during boot up. Typical operation is headless with interface through a serial port: this should still work, but video components on the carrier (if any) will be dark. Boot devices on the carrier, like MicroSd or SATA drives, will need driver code within the firmware to boot.

Some potential solutions for utilizing non-x86 SoCs in a COM Express environment could be:

1. Firmware that mimics many of the enumeration/configuration features of BIOS/EFI
2. Firmware that is built for a module in a specific carrier (note—this is a different from x86 modules and would prevent SoC-based modules from being shipped with “standard” firmware)
3. Firmware that does not initialize the carrier: carrier hardware may not be available during boot, O/S will have to initialize it

To standardize on the COM Express specification for non-x86 silicon, such differences in firmware behavior may need to be investigated for consideration.

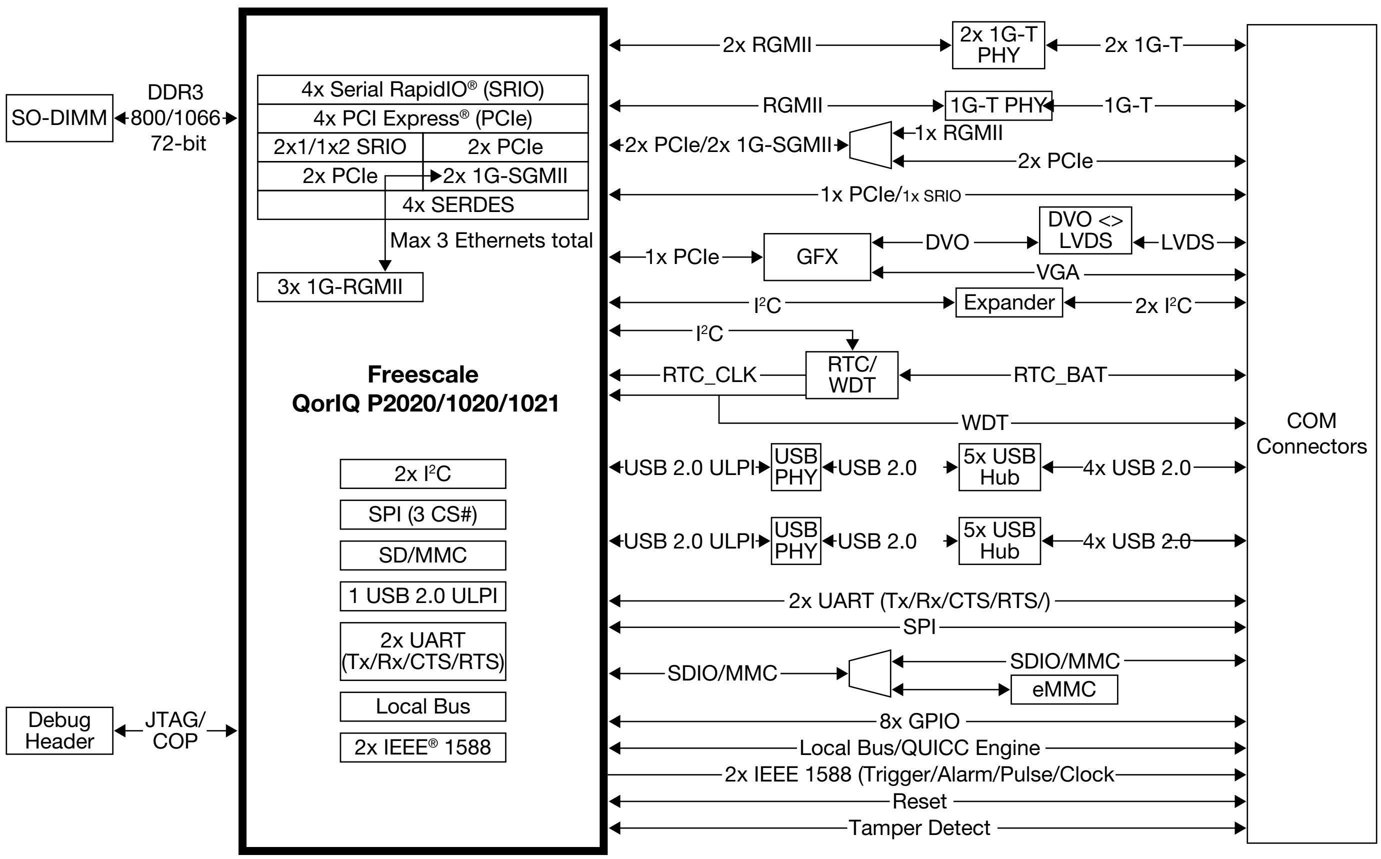
3 An example SoC-based COM Express board

This COM Express board concept, based on the Freescale QorIQ P2020, P1020, P1021 processors, contains a number of special interfaces not fully explored in this paper, including Local Bus, multiple I²C buses, DUARTs with flow-control and IEEE® 1588 clock signaling. This is intended to exemplify the variety of interfaces that should be considered and enabled by an SoC-oriented COM Express standard definition.

4 Wrap-up

The COM Express specification was initially targeted at x86 PC architecture processors and the form factor has gained market acceptance. We believe the general computer-on-module approach could be extended to apply more generically to SoC products as well. We would like to work together with the PICMG® organization to develop COM Express standards for non-x86 SoC processors.

Block Diagram Example: QorIQ P2020, P1020 or P1021 COM Express® Board



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