NTAG I<sup>2</sup>C plus Explorer Kit Peek and Poke

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#### Document information

Info	Content
Keywords	NTAG I <sup>2</sup> C plus, Explorer Kit, PC, NFC Tag, Peek and Poke
Abstract	This User Manual aims at describing the functionalities and how to use the Peek and Poke GUI together with the NTAG I <sup>2</sup> C <i>plus</i> Explorer Kit.



#### **Revision history**

Rev	Date	Description
2.1	20170925	Updated documentation with new features included in version 3.0 of Peek and Poke
2.0	20170315	Completely revised version
1.0	20151215	First version.

# **Contact information**

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## 1. Object



NTAG I<sup>2</sup>C *plus* Explorer kit is the first officially certified NFC Forum Type 2 Tag with I<sup>2</sup>C interface. It is an all-in-one demonstration and development resource to demonstrate the unique properties of the NTAG I<sup>2</sup>C *plus* tag chip. By including a full complement of hardware and software tools, users can not only investigate the capabilities of the chip through the various demonstrations, but also develop and test their own applications.

This User Manual explains how to use the Peek and Poke application for the new product of the NTAG family: NTAG I<sup>2</sup>C *plus*, which adds new features like password protection and originality signature.

Technical aspects related to the IC functioning (i.e. the configuration registers) are beyond the scope of this document. In order to get further technical details, please consult the dedicated Datasheet "NTAG I<sup>2</sup>C *plus*, NFC Forum Type 2 Tag compliant IC with I<sup>2</sup>C interface".

# 2. NTAG I<sup>2</sup>C *plus* introduction

The NTAG I<sup>2</sup>C *plus* is offering both contactless and contact interfaces. In addition to the passive NFC Forum compliant RF interface, the NTAG I<sup>2</sup>C *plus* product provides an I<sup>2</sup>C

interface that allows the IC to communicate with the microcontroller when the chip is powered by an external device, i.e. a mobile phone.

NTAG I<sup>2</sup>C *plus* operating in energy harvesting mode provides the possibility to supply external low power devices (e.g. microcontrollers) with the energy generated from the RF field of the external NFC device.



The NTAG I<sup>2</sup>C *plus* product has two types of memories:

- 1. EEPROM memory compliant with the NFC Forum Type 2 Tag implementation.
- 2. 64-byte SRAM memory, which is mapped with the EEPROM memory and is externally powered.

The NTAG I<sup>2</sup>C *plus* features a Pass-Through mode that allows fast download and upload of data from the RF interface to the I<sup>2</sup>C interface and vice versa. This functionality makes use of the SRAM memory that allows fast data transfer between interfaces without the EEPROM performance limitations.

In addition to the I<sup>2</sup>C interface functionality, the NTAG I<sup>2</sup>C *plus* product features an Event Detection Pin for waking up the host-connected devices or synchronizing the data transfer between the two interfaces.

The new NTAG I<sup>2</sup>C *plus* improves the last NTAG I<sup>2</sup>C version with some features such as FAST\_WRITE command and memory protection. The configuration of this memory protection field is explained in more detail in subsequent sections.

# 3. NTAG I<sup>2</sup>C plus Explorer kit contents

The NTAG I<sup>2</sup>C *plus* Explorer kit (NEK) consists of hardware and software tools that developers can use to understand the NXP NTAG I<sup>2</sup>C *plus* tag chip functionality and demonstrate its potential for other applications.

## 3.1 Hardware components

#### 3.1.1 NTAG I<sup>2</sup>C plus Explorer board

A hardware board based on the NXP LPC 11U24 32-bit ARM Cortex-M0 microcontroller, with on-board LCD display, NXP LM75B temperature sensor, voltage monitors, I<sup>2</sup>C serial bus connector, JTAG/SWD debug connector, RGB LED, micro USB connector and five push button controls.



#### 3.1.2 Antenna board

The antenna board carries the NTAG I<sup>2</sup>C plus 2k version itself and provides two interfaces:

- I. The RF interface to an NFC reader
- II. The I<sup>2</sup>C interface to the NTAG I<sup>2</sup>C *plus* Explorer board



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## 3.2 Peek and Poke GUI

The Peek and Poke GUI is a Windows application that can be used to examine the detailed memory contents of the NTAG I<sup>2</sup>C *plus* EEPROM via I<sup>2</sup>C interface. This software component is available as a download from the public NXP website.



# 4. NTAG I<sup>2</sup>C plus Peek and Poke GUI

The Peek and Poke application is a PC-based NTAG I<sup>2</sup>C and NTAG I<sup>2</sup>C *plus* exploration software tool with a graphical user interface. This software allows users to read from and write to the memory in the NTAG I<sup>2</sup>C *plus* chip via the I<sup>2</sup>C serial bus interface, as well as control the Session and Configuration registers.

Before working with the Peek and Poke GUI make sure your NTAG I<sup>2</sup>C Explorer Board is connected to your PC via USB.

### 4.1 GUI overview

Upon the start-up, the GUI overview is shown in Fig 6. Each region of the GUI is labeled for an easier reference. Each of these parts are the following:

- 1. The top bar contains most of the GUI controls.
- 2. The left column lists the NTAG I<sup>2</sup>C *plus* memory locations for each region indicated with the hexadecimal address.
- 3. The center grid displays the contents of those addresses in hexadecimal format.
- 4. The right column displays the ASCII representation of the data listed in the center column.

5. The bar at the bottom of the GUI indicates presence or absence of any connected NTAG I<sup>2</sup>C *plus* hardware and the status of the operations.

I <sup>®</sup> C Address Ste Block Read Block Writ	te All I	Read /	VI V	Inite N	DEF	Rese	et De	vice Ty	pe 1	NT3H2	111 (1	kB PI	us) •	400	kHz	*	-							NEC	Silence	e)		
k000: Configuration		0 1	2	3	4 5	5 6	5 7	8	9 /	A B	С	D	E	F .	0	1	2	3	4	5 6	7	8	9	A	в	C D	E	F
bd10: User memory (RW)	► 00	04 1	3 63	82	2E 4	IC 8	00 00	44	00	00 00	E1	10	6D (	00	1	1	c			L		D				á †	m	
x380: Dynamic lock bytes	01	63 5	F 91	02	35 5	53 7	0 91	01	14 3	54 02	65	6E	4E 1	54				1	5	S	p		1	T.,	3.	0 8	N	T
b380: Memory protection registers	02	41 4	7 20	49	32 4	13 2	45	58	50 14	IC 4F	52	45	52 1	51		G			2	0	- 6	X	P	L	0	RE	R	0
k3A0: Configuration registers	03	01 3	9 55	01	6E 7	78 7	0 2E	63	Œ 3	D 25	64	65	60 1	F		1	ы			<b>x</b> :	p	. e	0	m	1	d e	m	0
dF80: SRAM (R/W)	04	62 6	F 61	72	64 3	<b>F</b> 4	F 4D	35	35	36 39	-54	OF	13 1	61	b	•		. t	d.	1 1	0 M	- 8	5	8	9	T 8	1.1	-8
d'E0: Session registers	05	6E 6	A 72	6F	69 6	64 2	E 63	6F 1	60 3	3A 70	68	67	63 1	F		d	1	-0	1	d		0	80		p -	<u>k</u> g		-0
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## 4.2 GUI top control bar details

This section details each of the controls of the navigation bar on the top. See it depicted in Fig 7. The actions offered on this bar are: exporting and importing memory contents from or to a file, read and write to the memory, reset the memory to a default value, select the type of the device connected, scan for connected devices, setting of the device address and the selection of the speed of the bus for the communication. In addition, there is an information button about the application.

Version 3.0 of Peek and Poke includes 'NFC Silence' button, which implements NFC Silence feature for NTAG I<sup>2</sup>C *plus*. This button is described in more detail in a subsequent section.



## 4.2.1 Export / import memory contents

At the beginning of the navigation bar there are two icons to export and import the memory contents. They are shown in Fig 8, highlighted in red. The first folder icon is to open an HEX file containing a memory data and import it. The second icon, a disk, allows the user to export the data of the tables it into an HEX file.

NTAG I<sup>2</sup>C plus Explorer Kit Peek and Poke

 C Address
 Scan
 Write Block
 Read All
 Write NDEF
 Reset
 Device Type
 NT3H2211 (2 k8 Plus)
 100 kHz
 INFC Skience

 Fig 8.
 Peek and Poke import and export memory contents controls

### 4.2.2 Read and write controls

Read and write control buttons can be found at the top of the initial screen. Fig 9 shows the controls.

- *Write Block* button: Writes 16 bytes of data from the selected grid block into the tag.
- Read Block button: Reads 16 bytes of data and displays the contents on the grid.
- *Write All* button: Writes the entire EEPROM memory with the data on the grid into the tag.
- *Read All* button: Reads the entire EEPROM memory and displays it on the grid.



#### 4.2.3 Write NDEF message

The control *Write NDEF* opens a form with the option to enter a text and write it as an NDEF message or to write a default NDEF message. Fig 10 shows the control.

The default NDEF message is an NDEF SmartPoster composed of a Text message and a URI record (<u>Text record</u>: NTAG I2C Explorer, an <u>AAR</u>: android.com:pkgcom.nxp.ntagi2cdemo\_dev, and <u>URI record</u>: www.nxp.com/demoboard/OM5569).



Fig 11 shows the form with the two options to write a message and the tables with the message written and highlighted.

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#### 4.2.4 Reset tag memory

The reset button sets the NTAG I<sup>2</sup>C tag memory to the default value and displays it in the grid. The default tag memory value corresponds to a default NDEF message on the user memory (see structure in 4.2.3), and the default session and configuration register settings as defined in the NTAG I<sup>2</sup>C product datasheet. Fig 12 shows the control.



### 4.2.5 Device selection

The device selection allows us to change the device type. There are four possibilities here: the **NT3H1101** or **NT3H1201** (NTAG I<sup>2</sup>C, 1K and 2K) for the old NTAG I<sup>2</sup>C and **NT3H2111** or **NT3H2211** (NTAG I<sup>2</sup>C *plus* 1K and 2K) for NTAG I<sup>2</sup>C *plus*. The first and third options refer to the devices that have up to 1 kB of memory size, and the second and fourth ones refer to the 2 kB memory size. This is important because it will show a different grid depending on the memory size. Fig 13 shows the control.

In version 3.0, auto detection of tag is implemented. When the application detects that a new tag has been connected via USB, it automatically changes the device type and shows the corresponding memory map.



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#### 4.2.6 I<sup>2</sup>C device address and scanning

It is possible to change the I<sup>2</sup>C address of the NTAG I<sup>2</sup>C *plus* IC. Fig 14 shows the control. To change the default I<sup>2</sup>C address, a new value is needed in the text box. After click on the I<sup>2</sup>C Address button; once the button is clicked a new window will be prompted. This window will show the current I<sup>2</sup>C Address and a Textbox to insert the new Address. When the new address is written, it is necessary to click on 'OK' and then the new I<sup>2</sup>C address value is automatically written in the device. The default I<sup>2</sup>C serial bus address of the NTAG I<sup>2</sup>C tag chips is 0x55. I<sup>2</sup>C address is 7-bit. LSB bit designates the I<sup>2</sup>C Action – Read or Write to that address. While updating the 7 bit I<sup>2</sup>C address to block 0 byte 0 we have to left shift it by 1 bit and then write in Peek and Poke text box. For example, if we want an I<sup>2</sup>C address for NTAG to be 0x55h, value of 0xAAh which is (0x55 << 1) to the block 0 byte 0 needs to be written.

The Scan button will scan the entire range of possible addresses until it finds the device I<sup>2</sup>C address.



#### 4.2.7 I<sup>2</sup>C clock frequency

The I<sup>2</sup>C serial bus clock frequency can be changed by selecting a data rate from the dropdown. The maximum data rate supported by the tag is 400 KHz. Fig 15 shows the control.



#### 4.2.8 NFC Silence

When 'NFC Silence' button is active, the NFC silence feature is activated in the session registers of the NTAG I<sup>2</sup>C *plus*. This means that while the button is enabled it won't be possible to communicate with the tag via NFC. As it is only changed in the session registry, once the device is powered off the value will be reset.



## 4.3 Memory block selection

Another useful functionality of the Peek and Poke utility is given by its fluent and intuitive graphical exploration of the tag memory. As it was introduced in section 4.1, the application consists of three main panels. The left panel helps the user by selecting the memory sectors by the type of information they contain. This is done through a scroll tree menu allowing the user to explore a specific block or register. The center panel shows a grid structure that represents the hexadecimal content of the memory divided in blocks of 16 bytes. For the sake of a better understanding, the right panel displays the ASCII representation of the memory with the same structure.

Version 3.0 of Peek and Poke adds a more intuitive way to write values in the data grids. It is now possible to copy/paste 16 bytes (an entire row) of data, navigate to previous cells using the back-space key on the keyboard, or jump automatically to the next cell when a correct hex value is added in a cell.

When the user selects an item on the left menu, the specific sector is highlighted on the center and right panels to clearly identify the bytes devoted for that purpose. The content of a certain byte can be changed by modifying its value in the center panel and pressing either *Write Block* or *Write All*.

In the following subsections, the description of each node in the left panel is addressed.

#### 4.3.1 Configuration

The *Configuration* node in the left panel will highlight the first block of the memoryThe  $l^2C$  address byte can be changed through the dedicated button. (Section 4.2.6).

Expanding the *Configuration* node will show the five sections included in this block, allowing the user to identify the specific location for each of them.

If C Address Scan Write Block Read Block	Writ	te All	Rea	IIA t	Writ	e ND	EF	Reset	t D	evice	Тур	e NT	3H221	1 (2 )	kB PI	lus) •	1	00 kH	z •	0		2	VFC S	ilence								
Ox000: Configuration		0	1	2	3	4	5 6	3 7	7 8	9	A	В	С	D	E	F A	0	1	2	3	4	5	6	7	8	9	A	В	С	D	E	F
0x010: User memory (R/W)		00 0	A	AF	0A	07	4F 8	30 0	0 4	1 00	00	00	E1	10	6D	00		c	-			0			D					1	-	
0x380: Dynamic lock bytes		01 0	3 5F	91	02	35	53 7	70 9	91 0	1 14	54	02	65	6E	4E	54		-			÷.,	0			0		÷		a	- 45	m	
0x380: Memory protection registers		02 4	1 47	20	49	32 .	43 2	20 4	15 51	3 50	40	4F	52	45	52	51		-		1	5	S	р	-		4	Т	٦	0	n	N	T
<ul> <li>0x3A0: Configuration registers</li> </ul>		03 0	1 19	55	01	6E	78 7	70 2	E 63	3 6F	6D	2F	64	65	6D	6F =	A	G		1	2	с		E	X	P	L	0	R	E	R	Q
Dx400: User memory (R/W)		04 6	2 6F	61	72	64	2F 4	IF 4	ID 38	5 35	36	39	54	OF	13	61	1.2	r.	U		n	x	P	3	c	0	m	1	d	e	m	0
B 0xF80: SRAM (R/W)		05 6	E 64	72	6F	69	64 2	E 6	53 61	F 6D	) 3A	70	6B	67	63	6F	b	0	а	f	d	1	0	м	5	5	6	9	Т	X	1	а
OxFE0: Session registers		06 6	D 28	6E	78	70 :	2E 6	iE 7	74 6	1 67	69	32	63	64	65	6D	n	d	r	0	1	đ		c	0	m		P	k	9	c	0
		07 6	F FE	00	00	00	00 0	0 0	0 00	00 0	00	00	00	00	00	00	m		n	x	P		n	t	a	9	1	2	c	d	e	m
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		19 0	00 0	00	00	00	00 0	0 0	0 00	00 0	00	00	00	00	00	00																

#### 4.3.2 User memory

The *User Memory* node shows the content of the tag user memory in the central and right panels. The tree structure in this case allows the user to locate a specific block of the user memory. All this content is completely editable through the center panel interface.

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With the new features of the NTAG I<sup>2</sup>C *plus,* it is possible to protect some parts of the memory against I<sup>2</sup>C (not only NFC). Fig 19 displays the reading of the user memory with this protection active. The protected area is shown in orange and the unprotected in green.



### 4.3.3 Dynamic lock bytes

In order to observe the dynamic lock bytes, click on *Dynamic lock bytes* in the left panel. In the middle and right panel, one block highlighted in green should appear, which shows the memory position of the dynamic lock bytes.

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#### 4.3.4 Memory protection registers

This field is introduced in the NTAG I<sup>2</sup>C *plus* release. It will display all options of the access registers. Fig 21 shows this new feature. In the left panel the main registers are defined and by clicking on any of them, the middle and right panel should highlight the corresponding block.

I <sup>2</sup> I <sup>2</sup> C Address Scan Write Block Read Block	Write A	AL F	lead Al	W	rite N	DEF	Res	et	Devi	ice T	ype I	NT3	42211	(2 kB	Plus)		1	.00 kł	iz •	Û			NFC S	ilence							
0x000: Configuration		0	1 2	3	4	5	6	7	8	9	A I	в	C D	Е	F	*	0	1	2	3	4	5	6	7	8	9	A	В	c r	E	F
- 0x000: IPC address (W)	2A	00	00 0	00 (0	00	00	00	00	00	00	00 (	00	00 00	00	00																
- 0x001: Serial Number (R)	2B	00	00 0	00	00	00	00	00	00	00	00 1	00	00 00	00	00																
- 0x007: Internal data (R)	20	00	00 0	00 00	00	00	00	00	00	00	00 4	00	00 00	00	00																
0x00A: Lock bytes (R/W)	2D	00	00 0	00 (	00	00	00	00	00	00	00 4	00	00 00	00	00																
- 0x00C: Capability Container (R/W)	2E	00	00 0	00 00	00	00	00	00	00	00	00 (	00	00 00	00	00																
0x010: User memory (R/W)	2F	00	00 0	00 0	00	00	00	00	00	00	00 0	00	00 00	00	00																
0x380: Dynamic lock bytes	30	00	00 0	00 (0	00	00	00	00	00	00	00 1	00	00 00	00	00																
0x380: Memory protection registers	31	00	00 0	00 00	00	00	00	00	00	00	00 0	00	00 00	00	00																
0x3A0: Configuration registers	32	00	00 0	00	00	00	00	00	00	00	00 (	00	00 00	00	00																
0x400: User memory (R/W)	33	00	00 00	3 00	00	00	00	00	00	00	00 4	00	00 00	00	00	in l															
0xF80: SRAM (R/W)	34	00	00 0	00 (0	00	00	00	00	00	00	00 (	00	00 00	00	00																
0xFE0: Session registers	35	00	00 00	00 00	00	00	00	00	00	00	00 0	00	00 00	00	00																
	36	00	00 0	00	00	00	00	00	00	00	00 0	00	00 0	00	00	-															
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	3A	01	07 F	8 48	08	01	00	00	00	00	00 4	00	00 00	00	00			•	ø	н											
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	42	00	00 0	00	00	00	00	00	00	00	00 (	00	00 00	00	00																
	43	00	00 0	00 00	00	00	00	00	00	00	00 4	00	00 00	00	00																
	44	00	00 0	00 (	00	00	00	00	00	00	00 4	00	00 00	00	00																
	45	00	00 0	00 00	00	00	00	00	00	00	00 (	00	00 00	00	00																
Session Confin Accorn	46	00	00 0	00 00	00	00	00	00	00	00	00 0	00	00 00	00	00																
Registers Registers Registers	47	00	00 0	00 00	00	00	00	00	00	00	00 (	00	00 00	00	00																
	48	00	00 0	00 00	00	00	00	00	00	00	00 0	00	00 00	00	00																

### 4.3.5 Configuration registers

You can also observe the configuration registers by clicking on *Configuration registers* in the left panel. In the middle and right panel, one block highlighted in green should appear, which shows the memory position of the configuration registers.

**UM10967** 

S In I C Address Scan Write block Read block	Write A	11 14	Read Al	N	/rite N	IDEF	Res	set	Dev	ice Ty	ype I	NT3F	12211	(2 kB	Plus)	•	1 10	00 kH	z •	U		1	VFC S	dence	•							
0x000: Configuration		0	1 2	3	4	5	6	7	8	9	A	B	C D	E	F	*	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E I	F
0x000: I <sup>2</sup> C address (W)	2A	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
- 0x001: Serial Number (R)	2B	00	00 00	0 01	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0x007: Internal data (R)	20	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
- 0x00A: Lock bytes (R/W)	2D	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
- 0x00C: Capability Container (R/W)	2E	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0x010: User memory (R/W)	2F	00	00 00	0 00	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0x380: Dynamic lock bytes	30	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0x380: Memory protection registers	31	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0x3A0: Configuration registers	32	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0x400: User memory (R/W)	33	00	00 00	0	00 0	00	00	00	00	00	00	00	00 00	00	00	in l																
0xF80: SRAM (R/W)	34	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
0xFE0: Session registers	35	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	36	00	00 00	0 01	00 0	00	00	00	00	00	00	00	00 00	00	00	-																
	37	00	00 00	0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	38	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	FF																	3
	39	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	► 3A	01	07 F	3 4	3 08	01	00	00	00	00	00	00	00 00	00	00			٠	ø	н												
	40	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	41	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	42	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	43	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	44	00	00 00	0 00	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	45	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
Ounter Auren	46	00	00 00	0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
Registers Registers Registers	47	00	00 00	0	00 0	00	00	00	00	00	00	00	00 00	00	00																	
	48	00	00 00	0 0	00 0	00	00	00	00	00	00	00	00 00	00	00																	

#### 4.3.6 SRAM

To see the SRAM bytes you have to click on *SRAM* in the left panel. The middle and right panel several blocks highlighted in green should appear, which show the memory positions of the SRAM.

I <sup>C</sup> Address Scan Write Block	Read Block	Write All	Rea	d All	Wri	te ND	DEF	Rese	t De	vice	Type	NT3	H21	11 (1	kB PI	us) •	40	0 kH	z		2	_	-	_			_	_	NEC	Silen	ce			_
0x000 Configuration	- Production of the		0	1		4	4 . 4				0		0	0	0						2	3	4	6	0	7	0	0	A	P	0	D		5
0x010: User memory (RW)			00	00	00	00 1	00 0	0 0/	, 00	00	00	00	00	00	00	00	00	IF	-	-	*		-		0	·:			~		<i>w</i>		÷	
0x380: Dynamic lock bytes		20	00	00	00	00 0	00 0	0 00	0 00	00	00	00	00	00	00	00	00	Ш.																
0x380: Memory protection registers		23	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
0x3A0: Configuration registers		25	00	00	00	00 1	00 00	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
0xF80: SRAM (R/W)		26	00	00	00	00 1	00 00	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
Od/E0: Session registers		27	00	00	00	00 1	00 00	0 00	0 00	00	00	00	00	00	00	00	00	Ш.																
		28	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		29	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		24	00	00	00	00 1	00 00	0 00	0 00	00	00	00	00	00	00	00	00	Ш.																
		28	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	Ш.																
		20	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		20	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		2E	00	00	00	00 1	00 00	0 00	00 0	00	00	00	00	00	00	00	00	Ш.																
		2F	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	Ш.																
		30	00	00	00	00 0	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		31	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	н.																
		32	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	н.																
		33	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	н.																
		34	00	00	00	00 0	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		35	00	00	00	00 1	00 00	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		36	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																
		37	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00	ш.																1
	(	38	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	5 1																	y
Session Config Registers Registers	Access Remeters	39	00	00	00	40 1	00 0	0 0	0 00	00	00	00	00	00	00	00	00	н.			-		-											
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you want to get Logging information you can use	any freeware tool	- 1 18	00	00	00	00 0	00.0			00	00	00	00	00	00	00	00																	
e https://www.hhdsoftware.com/		54	00	00	00	00 1	00 0	0 00	0 00	00	00	00	00	00	00	00	00																	
		100	00	00	00	00	00 0	0 00	0 00	00	00	00	00	00	00	00	00																	
		FE	01	07	FB	48 1	08 0	1 00	0 00	00	00	00	00	00	00	00	00 -	11		•	0	н		_				_	_					
dec	TAG I <sup>2</sup> C hardware	detected	-														abata 12	100	-	-	-	Description of		-	-	-	-	-	_	_	-		-	-
177 SUCCASE 51	TALLS IN THE PROPERTY OF THE P																																	

#### 4.3.7 Session registers

In order to observe the session registers you can click on *Session registers* in the left panel. In the middle and right panel, the last block highlighted in green should appear, which shows the memory position of the session registers. There is also special access button which opens special window to configure Session registers, described in 4.4.2 Session registers.

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🥁 🚽 I <sup>a</sup> C Address Scan Write B	lock Read Block	Write All	Read	All	Write	NDEF	Re	eset	Dev	ice Ty	pe	NT3H	2111	(1 k8	Plus)	•	400 1	kHz	-	0	-				-	-	N	FC Sile	ence		-	
0x000: Configuration			0	1	2 3	4	5	6	7	8	9	A E	1 0	: D	E	F	-	0	1	2	3	4	5	6	7	8	9 A	в	С	D	E	F
Ck010: User memory (R/W)		22	00	00	00 00	00	00	00	00	00 0	00	00 0	0 0	0 00	00	00																
0x380: Dynamic lock bytes		23	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
0x380: Memory protection registers		24	00	00	00 00	00	00	00	00	00 (	00	00 0	0 0	0 00	00	00																
0x3A0: Configuration registers		25	00	00	00 00	00	00	00	00	00 1	00	00 0	0 0	0 00	00	00																
DvF80: SRAM (R/W)		26	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
DdFE0: Session registers		27	00	00	00 00	00	00	00	00	00 (	00	00 0	0 0	0 00	00	00	3.11															
		28	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
		29	00	00	00 00	00	00	00	00	00 (	00	00 0	0 0	0 00	00	00																
		2A	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
		28	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00	11															
		2C	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
		2D	00	00	00 00	00	00	00	00	00 1	00	00 0	0 0	0 00	00	00		-														
		26	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
		2F	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 0	00	00	11															
		30	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00		-														
		31	00	00	00 00	00	00	00		00	00	00 1	u .	0 0	00	00		- I														
		32	00	00	00 00	00	00	00	00	00 1	00	00 0	0 0	0 0	00	00																
		33	00	00	00 00	00	00	00	00	00 1	00	00 0	0 0	0 0	00	00																
		39	00	00	00 00	00	~	00	00	00	~	00 0		0 0	- 00	00																
		30	00	00	00 00	00	00	00	00	00	00	00 0	0 0	10 0	00	00		-														
		30	00	00	00 00	00	00	00	00	00 1	00	00 0	0 0	0 0	00	00		-														
		- 38	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	FF	11															ÿ
Session Config	Access	39	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																1
Registers Registers	Registers	34	41	07	F8 48	08	01	00	00	00	00	00 0	0 0	0 00	00	00		A			н											
		F8	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00																
you want to get Logging information you ca	n use any freeware tool	F9	00	00	00 00	00	00	00	00	00 (	00	00 0	0 0	0 00	00	00																
ke https://www.hhdsoftware.com/		EA	00	00	00 00	00	00	00	00	00	00	00 0	0 0	0 00	00	00	111															
		FB	00	00	00 00	00	00	00	00	00	00	00 0	0 0	00 00	00	00																
		> FE	01	07	F8 48	08	01	00	00	00	00	00 0	0 0	10 00	00	00	-		•	0	н								11		1001	
de e	NTAG PC hardware																															

## 4.4 GUI bottom control bar details

## 4.4.1 USB data logging

The data that is transmitted over the USB connection can be tracked. Any freeware tool available online shall suffice.

Note: USB data logging affects the amount of time required to read / write.

#### 4.4.2 Session registers

The user can check and edit the session registers by clicking the address 0xFE or the *Session Register* button. For a quick explanation for any of the registers listed under the session and configuration register screens, click on the small blue information (*i*) icon. This action will bring up a help screen describing the register in a bit more detail.



For more information on the session registers, please go to the NTAG I<sup>2</sup>C plus datasheet.

## 4.4.3 Configuration registers

The user can check and edit the configuration registers. Press the configuration register button at the bottom left of the screen or click on the grid at memory block 0x3A for NTAG I<sup>2</sup>C 1K or 0x7A for NTAG I<sup>2</sup>C 2K. For a quick explanation of a session or configuration register, click on the small blue information (*i*) icon. This action will bring up a help screen describing the register in a bit more detail.

I <sup>2</sup> C Address	Scan Write Block Read Block	Write All Read All Write NDEF Reset Device Type NT3H2211 (2 kB Plus) + 100 kHz + 👔 NFC Silence	
0x000: Configuration     0x000: PC address     0x001: Serial Numb	Configuration Registers	0 1 2 3 4 5 6 7 8 9 A B C D E F A B C D E F A B C D E F A B C D E F A B C D E F A B C D B C D E F A B C D C D C C C C C C C C C C C C C C C	E F
-Dx007: Internel date -Dx00A: Lock bytes ( -Dx00C: Capability C ⊕x010: User memory ( ⊕x380: Dynamic lock b ⊕x380: Memory protec	NC_REG: 0x3A0 NFCS_I2C_RST_ON_OFF PTHRU_ON_OFF FD_OFF 00: Field switched off	LAST_NDEF_BLOCK_0dA1 WDT_odA(13) 0 4 5 5 6 9 T 1 4 1 4 1 4 1 4 1 4 1 4 1 4 1 4 1 4 1	m o ‼ a c o e m
0x3A0: Configuration r     0x400: User memory (P     0xF80: SRAM (R/W)     0xFE0: Session registe	FD_ON 00: Field presence SRAM_MIRROR_ON_OFF TRANSFER_DIR	SRAM_MIRROR_BLOCK.buA2         REG_LOCK.buA4         00           IPC block address         F8         IPC_LOCKED         00           IPC block address         F8         IPC_LOCKED         00	
	IZC_CLOCK_STR: 0x3A-5	00 Write Config Read Config 00 Close 00	
Session Registers	Config Registers Registers	17       00 <td< td=""><td></td></td<>	

For more information about the configuration registers, please go to the NTAG I<sup>2</sup>C *plus* datasheet.

### 4.4.4 Access configuration registers

It is possible to read and write the new access registers introduced in the NTAG I<sup>2</sup>C *plus*. Pressing the Access registers button at the bottom left of the screen will display the window where it is possible to read and write these values. For a quick explanation of a session or configuration register, click on the small blue information (*i*) icon. This action will bring up a help screen describing the register in a bit more detail.

Note the warning text is highlighted in red. This warning concerns the writing and reading PWD and PACK fields. When these fields are read, it won't show the real value. These fields will be read as all zeros (00000000 for PWD and 0000 for PACK).

When writing these fields, it is important to keep in mind that the values shown in the text boxes will be written (the configuration shown in the Fig 27 will write 00000000 as PWD), so if the tag is going to become protected it is important to realize that this tag is going to be protected with that password. Note, that PC and Android app use as default password SUN = 0xFFFFFFFF, STAR = 0x555555555 and MOON = 0xAAAAAAAA.

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8 H	I <sup>2</sup> C Address	Scan	Write Block	Read Block	Write All	Read All	Write I	NDEF	Reset	Devio	е Туре	NT	BH221	l1 (2 k	B Plus	i) •	1	.00 kł	łz ۰	0		NF	C Silena	.0						
0x000 C	Configuration	AFC.				1 1 2	3 4	.5	6.7	8 9	A	B	C	DI	E F	*	0	1	2	3	4	5 6	7	8	9	A	вс	D	E	F
0x00 0x00 0x00 0x00 0x380 0x380 0x380 0x380 0x400 0xFE0	AUTH0 AUTH0 AUTH0 PWD Password The fields Pi and always i Be aways i	FF FFFFFFFF VD and PAC eturns 00.00	K cannot be rea	ACCESS AUTHU NFC, NFC, W	S M 0 DIS_SEC1 PROT rite Access sed Access	]	PT_I2C	: PROT ROT 00: Entr	0 T e memoi 000	•	54 4C 6D 36 3A 69 00 00 00 00 00 00 00 00 00 0	02 4F 2F 39 70 32 00 00 00 00 00 00 00 00 00 00 00	65 52 64 54 68 63 00 00 00 00 00 00 00 00 00 00 00	45         45           65         6           67         6           67         6           64         6           00         0           00         0           00         0           00         0           00         0           00         0           00         0           00         0           00         0           00         0           00         0           00         0           00         0	He         SH           S2         51           SD         6F           I3         61           I4         00           I5         60           I5         60           I5         60           I5         60           I5         60           I5         60           I6         00           I6         00           I6         00           I6         00           I6         00	1 F F D D D D D D D D D D D D D D D D D	A	-G+od-p	U a r n	T T O X	s n d i P	3   C   X   J   d	E D M c t	X 5 0 a	1 P 5 m 9	L m 6 :	1 0 1 9 7 9 1 2 1	a n R E I e R X G C d	R m II c e	Q o a o m
Sessic Registe	are overwrit	Config Registers	Ar	ccess	12 0 13 0 14 0 15 0 16 0 17 0 18 0 19 0	0 00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00 00	00 0 00 0 00 0 00 0 00 0 00 0 00 0 00	00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00		00         00         00           00         00         00           00         00         00           00         00         00           00         00         00           00         00         00           00         00         00           00         00         00           00         00         00           00         00         00	) ) ) ) ) ) ) )														

For more information about the configuration registers, please go to the NTAG I<sup>2</sup>C Datasheet.

## 4.5 HID Library EULA

As this application uses an external library for HID devices, the corresponding End User License Agreement is added below:

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User manual

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