TN00005

Migration from LPC1100L to LPC1100XL

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Document information

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Abstract	This technical note introduces the features of the LPC1100XL series, and details the differences when compared to the LPC1100L series. This technical note will help enable users to have a smooth migration process from the LPC1100L series to the LPC1100XL series.

Revision history

Rev	Date	Description
1	20120305	Initial version.

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1. Introduction

The LPC111x/LPC11Cxx are an ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC111x/LPC11Cxx operate at CPU frequencies of up to 50 MHz. The peripheral complement of the LPC111x/LPC11Cxx includes up to 32 kB of flash memory, up to 8 kB of data memory, one C_CAN controller (LPC11Cxx), one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 UART, up to two SPI interfaces with SSP features, four general purpose timers, a 10-bit ADC, and up to 42 general purpose I/O pins.

On-chip C_CAN drivers and flash In-System Programming tools via C_CAN are included on the LPC11Cxx. In addition, parts LPC11C2x are equipped with an on-chip CAN transceiver.

The LPC111x/LPC11Cxx consists of the following family series:

- LPC1100 series
- LPC1100L series
- LPC1100XL series
- LPC11C00 series
- LPC11D14 series

This technical note introduces the important features of the LPC1100XL series, and focuses on providing key differences which users must be aware of in order to have a smooth migration process from the LPC1100L series to the LPC1100XL series.

The user software on the LPC1100L series is fully portable to the LPC1100XL series if the part IDs and/or the Device ID register are not used in the LPC1100L user software.

The various topics covered in this application note are as follows:

- Flash memory size
- Flash sector configuration
- 16-bit and 32-bit timer peripherals
- Pin configuration
- Device identification register
- Part identification numbers
- Non-Maskable Interrupt (NMI)
- Power consumption
- Summary

2. Flash memory size

For the LPC1100L series, the maximum on-chip flash memory size available is 32 kB. For the LPC1100XL series, the maximum on-chip flash memory size available is 64 kB.

3. Flash sector configuration

For the LPC1100L series, the on-chip flash memory consists of sectors where each sector size is 4 kB. Please see Fig 1:

Sector number	Sector size [kB]	Address range
0	4	0x0000 0000 - 0x0000 0FFF
1	4	0x0000 1000 - 0x0000 1FFF
2	4	0x0000 2000 - 0x0000 2FFF
3	4	0x0000 3000 - 0x0000 3FFF
4	4	0x0000 4000 - 0x0000 4FFF
5	4	0x0000 5000 - 0x0000 5FFF
6	4	0x0000 6000 - 0x0000 6FFF
7	4	0x0000 7000 - 0x0000 7FFF

Fig 1. LPC1100L flash sector configuration

The LPC100L series provides IAP erase operations only on a sector basis and the minimum erase size available is 4 kB. The IAP erase sector command code 52 (decimal) can be used to erase a sector or multiple sectors of the on-chip flash memory. Please see the LPC11xx/LPC11Cxx user manual for further details.

For the LPC1100XL series, the on-chip flash memory consists of sectors where each sector size is 4 kB, and each sector consists of 16 pages. Each page is 256 bytes. Please see Fig 2:

Sector number	Sector size [kB]	Page number	Address range
0	4	0 -15	0x0000 0000 - 0x0000 0FFF
1	4	16 - 31	0x0000 1000 - 0x0000 1FFF
2	4	32 - 47	0x0000 2000 - 0x0000 2FFF
3	4	48 - 63	0x0000 3000 - 0x0000 3FFF
4	4	64 - 79	0x0000 4000 - 0x0000 4FFF
5	4	80 - 95	0x0000 5000 - 0x0000 5FFF
6	4	96 - 111	0x0000 6000 - 0x0000 6FFF
7	4	112 - 127	0x0000 7000 - 0x0000 7FFF
8	4	128 - 143	0x0000 8000 - 0x0000 8FFF
9	4	144 - 159	0x0000 9000 - 0x0000 9FFF
10	4	160 - 175	0x0000 A000 - 0x0000 AFFF
11	4	176 - 191	0x0000 B000 - 0x0000 BFFF
12	4	192 - 207	0x0000 C000 - 0x0000 CFFF
13	4	208 - 223	0x0000 D000 - 0x0000 DFFF
14	4	224 - 239	0x0000 E000 - 0x0000 EFFF
15	4	240 - 255	0x0000 F000 - 0x0000 FFFF

Fig 2. LPC1100XL flash sector configuration

Compared to the LPC1100L series, the LPC1100XL series provides IAP erase operations on both sector and page basis. As a result, the minimum erase size available is 256 bytes on the LPC1100XL. The IAP erase page command code 59 (decimal) can be used to erase a page or multiple pages of the on-chip flash memory. Please see the LPC11xx/LPC11Cxx user manual for further details.

4. 16-bit and 32-bit timer peripherals

Compared to the LPC1100L, the LPC1100XL series provides the following additional features on the 16-bit Timer 0/1 and 32-bit Timer 0/1 peripherals:

1. One additional capture input signal for each timer:
   - CT16B0_CAP1
   - CT16B1_CAP1
   - CT32B0_CAP1
   - CT32B1_CAP1

Please see Fig 3 for the signal location.

2. Capture-clear function for easy pulse-width measurement.

This feature allows for a designated edge on a particular CAP input to reset the timer to all zeros. Using this mechanism to clear the timer on the leading edge of an input pulse and performing a capture on the trailing edge permits direct pulse-width measurement using a single capture input without the need to perform a subtraction operation in software.

Bits 7:4 of the Counter Control Register are used to enable and configure the capture clears-timer feature. Please see the LPC11xx/LPC11Cxx User Manual for further details.

5. Pin configuration

The LPC1100XL series is fully pin to pin compatible with the LPC1100L series. Compared to the LPC1100L series, the LPC1100XL series multiplexes the following signals on additional general purpose port pins.

- SCK1 - Serial clock for SPI1
- MISO1 - Master In Slave Out for SPI1
- MOSI1 - Master Out Slave In for SPI1
- SSEL1 - Slave Select for SPI1
- RXD - Receiver input for UART
- TXD - Transmitter output for UART
- CT16B0_CAP0 - Capture input 0 for 16-bit timer 0
- CT16B0_MAT0 - Match output 0 for 16-bit timer 0
- CT16B0_MAT1 - Match output 1 for 16-bit timer 0
- CT16B0_MAT2 - Match output 2 for 16-bit timer 0
- CT16B1_MAT1 - Match output 1 for 16-bit timer 1
- CT32B0_CAP0 - Capture input 0 for 32-bit timer 0
- CT32B0_MAT0 - Match output 0 for 32-bit timer 0
- CT32B0_MAT1 - Match output 1 for 32-bit timer 0
- CT32B0_MAT2 - Match output 2 for 32-bit timer 0
- CT32B0_MAT3 - Match output 3 for 32-bit timer 0

Fig 3 and Fig 4 highlights the location of these functions on the LPC1100XL series.

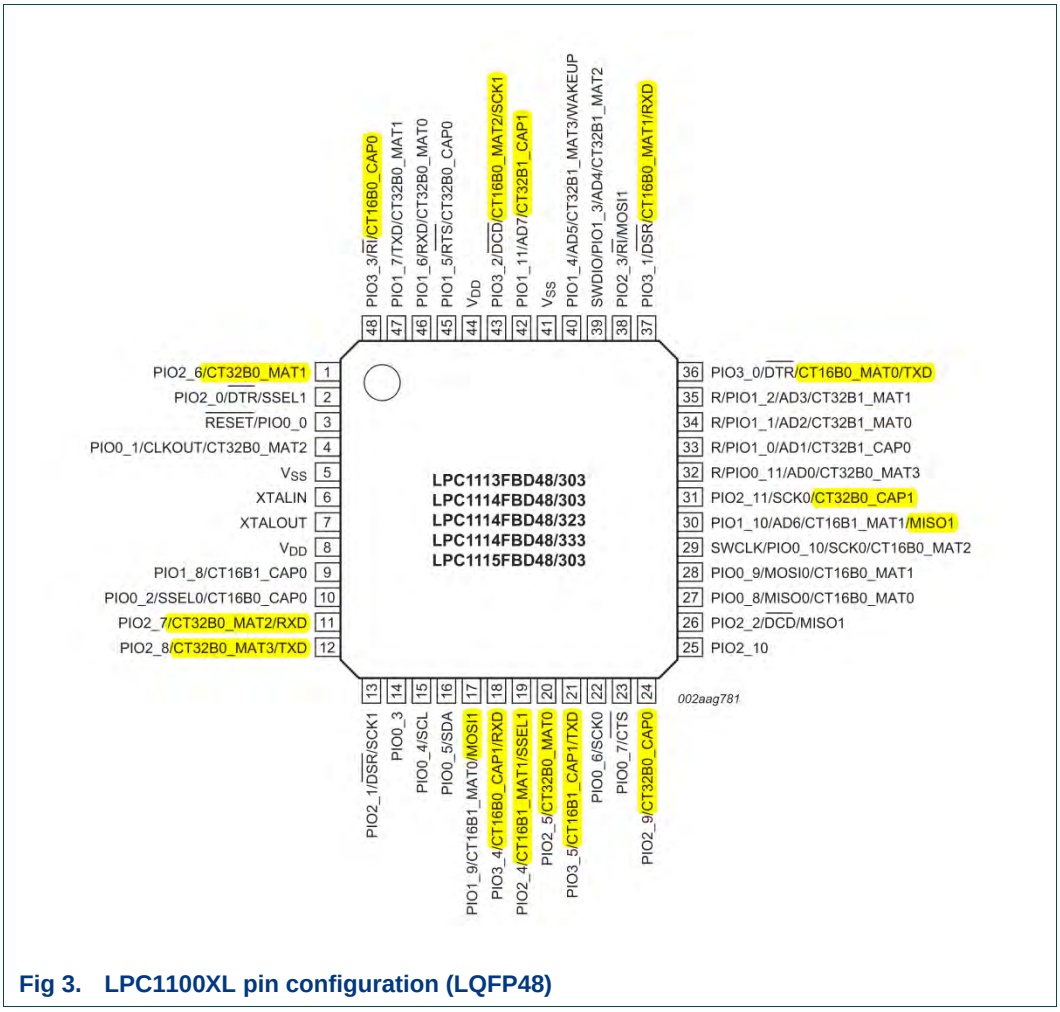

Fig 3. LPC1100XL pin configuration (LQFP48)

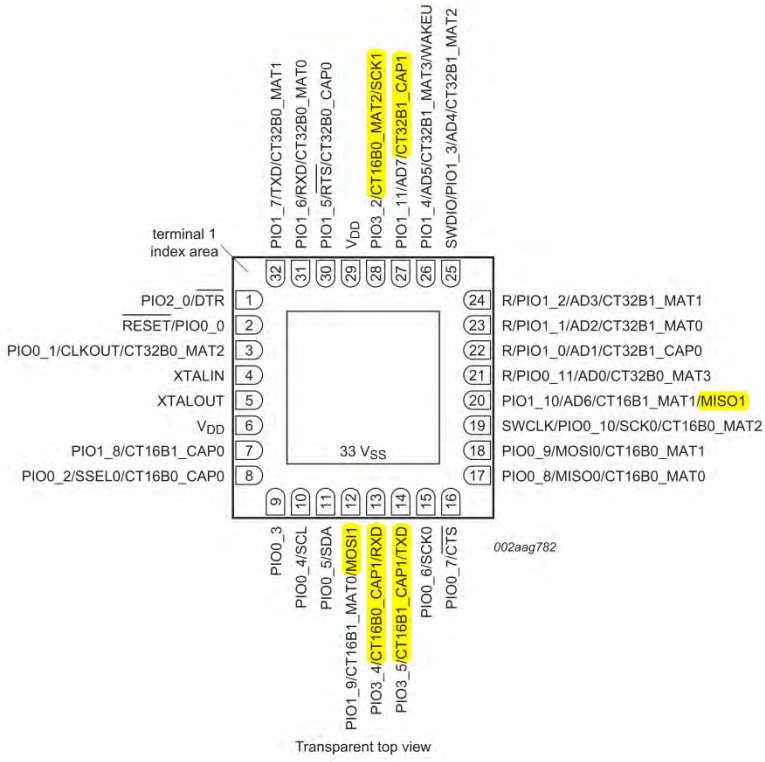

Fig 4. LPC1100XL pin configuration (HVQFN33)

6. Device identification register

On the LPC1100L series, the device identification register which is available in the SYSCON block (address 0x400483F4) is a read-only register and contains the part identification numbers for the parts.

On the LPC1100XL series, the device identification register is not supported. The part identification numbers for the parts can only be read using the IAP Read Part Identification command or the ISP Read Part Identification command. Please see the LPC11xx/LPC11Cxx user manual for further details.

7. Part Identification numbers

The part ID numbers for the LPC1100XL parts have different part ID numbers compared to the LPC1100L parts.

As mentioned above, the part IDs for the LPC1100XL parts can only be read using the IAP Read Part Identification command or the ISP Read Part Identification command. Please see the LPC11xx/LPC11Cxx user manual for further details.

8. Non-Maskable Interrupt (NMI)

On the LPC1100XL series, a non-maskable interrupt source has been added where the peripheral interrupts can be selected as a source for the NMI interrupt of the ARM Cortex-M0. This is the highest priority exception other than reset and it cannot be masked or prevented from activation by any other exception.

This is enabled via the NMI source register (NMISRC, 0x40048174). Please see the LPC11xx/LPC11Cxx user manual for further details.

9. Power consumption

The LPC1100XL series has been designed to provide lower power consumption. Compared to the LPC1100L series (130 uA/MHz), the LPC1100XL series provides 110 uA/MHz (typical) in active mode, and in addition, the deep sleep current is typically 1.8 uA (2 uA on the LPC1100L).

Please see the LPC1100L and LPC1100XL datasheets for a detailed comparison on the power consumption numbers.

10. Summary

The following table summarizes the differences between the LPC1100XL and LPC1100L series.

Table 1. LPC1100XL and LPC1100L feature differences

LPC1100XL	LPC1100L
110 uA/MHz (typical) Power Consumption	130 uA/MHz (typical) Power Consumption
110 uA/MHz (typical) Power Consumption	130 uA/MHz (typical) Power Consumption
1.8 uA Deep Sleep Current (Typical)	2.0 uA Deep Sleep Current (Typical)
IAP Sector Erase (4 kB) and IAP Page Erase (256 Bytes)	IAP Sector Erase (4 kB)
64 kB Flash Memory	32 kB Flash Memory
Non Maskable Interrupt	-
One capture function added for each timer.	-
Capture-clear feature on the 16-bit and 32-bit timers for easy pulse-width measurements.	-
Timer, UART, and SSP functions pinned out on additional GPIO pins.	-
-	Device ID Register
Part Identification Numbers (Please see the LPC11xx/LPC11 User Manual)	Part Identification Numbers (Please see the LPC11xx/LPC11 User Manual)

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