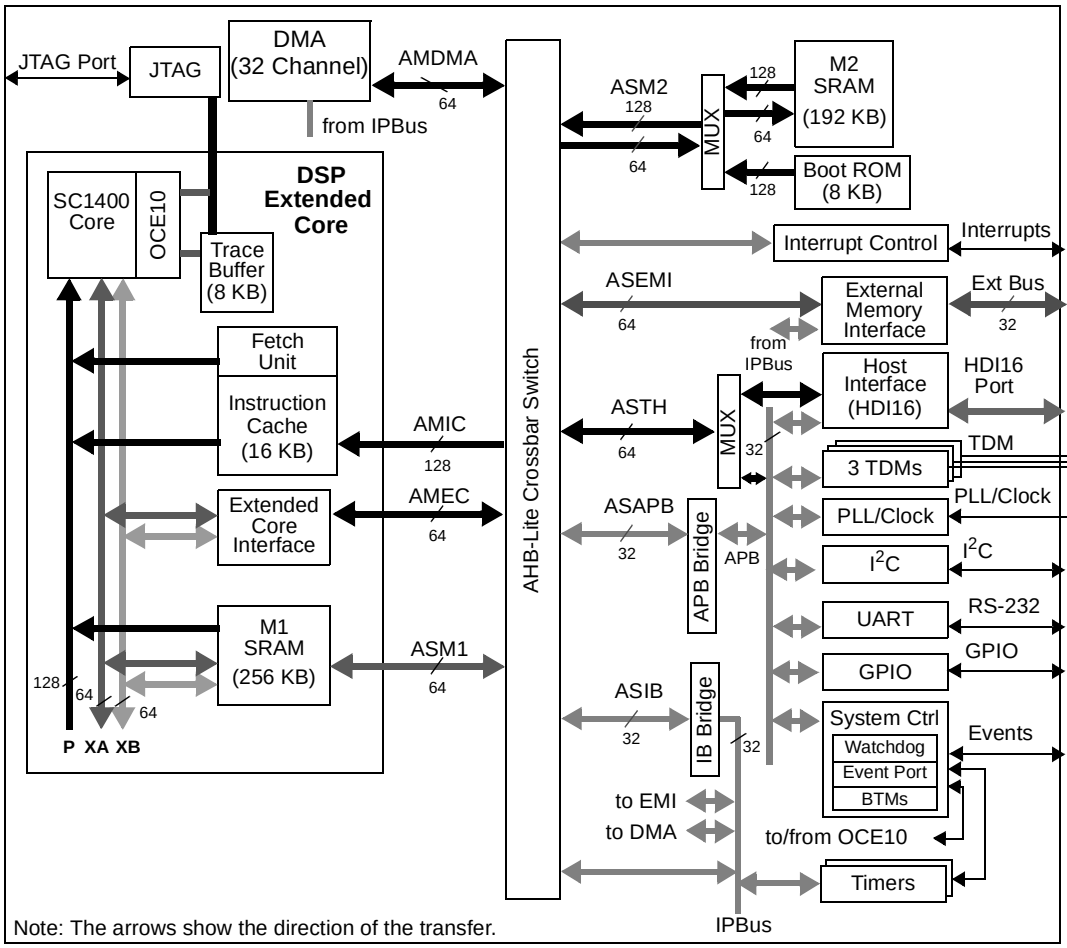
MSC7118

Low-Cost 16-Bit DSP With DDR Controller



The MSC7118 device targets high-bandwidth highly computational DSP applications and is optimized for Enterprise class packet telephony applications, providing a competitive price per channel for voice-over-packet systems.

The MSC7118 device is a member of the Freescale MSC711x family, a high-performance, cost-effective family of DSPs based on the StarCore ™ SC1400 core that offers system solutions, flexibility with peripherals and performance, and overall system cost savings. Devices in the MSC711x family target high-bandwidth highly computational DSP applications and are optimized for packet telephony applications, providing a competitive price per channel for voice over packet systems. The MSC7118 is a highly integrated DSP that contains the SC1400 core, on-chip emulation logic, 448 KB of SRAM memory, 16 KB ICache, 8 KB boot ROM, 8 KB trace buffer, a 32-channel DMA controller, a 4-layer crossbar switch, a DDR memory controller, three 128-channel time-division multiplexing (TDM) interfaces with hardware support for µ/A-law decoding/encoding, a UART, a 16-bit host interface (HDI16) to support an external host processor, a programmable interrupt controller (PIC), an I^2C interface, eight timers, GPIO signals, and a JTAG port. The SC1400 core has four ALUs and performs at 1200 DSP million multiply accumulates per second (MMACS) with an internal 300 MHz clock at 1.2 V.

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Features

Table 1 lists the features of the Freescale MSC7118 device.

Table 1. MSC7118 Features

Feature	Description
Extended Core	
SC1400 Core	• Up to 1200 MMACS using an internal 300 MHz clock at 1.2 V. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update. • 4 data ALUs. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • JTAG test access port designed to comply with **IEEE®** Std. 1149.1™. • On-chip emulator (OCE10) module with real-time debugging capabilities: – 6 address breakpoint units. – 1 data breakpoint unit. – 8 KB trace buffer. – 62-bit counter. – On-chip emulator transmit and receive registers.
Extended Core	The high performance extended core delivers up to 1200 MMACS using 4 ALUs running up to 300 MHz, including: • SC1400 core processor. • 256 KB memory space (M1) accessed by the SC1400 core with no wait states and atomic access support. • 16 KB, 16-way instruction cache (ICache). • Programmable instruction fetch unit. • Write buffer (4 locations). • Extended core interface module.
Internal Memory	The large internal memory space totals 448 KB: • 256 KB of M1 memory. • 192 KB internal shared memory (M2), accessible from the extended core instruction fetch unit, extended core interface, and DMA controller via the crossbar switch. • 16 KB ICache. • 8 KB boot ROM accessible from the SC1400 core.
Data Transfer System	
Crossbar Switch	AHB-Lite crossbar switch, allowing up to four parallel data transfers between four master ports and six slave ports, where each port connects to an AHB-Lite bus: • Fixed or round robin priority independently programmable at each slave port. • Programmable bus parking at each slave port. • Low-power mode.
DMA Controller	Multi-channel DMA controller: • Up to 32 time-multiplexed channels. • Priority-based time-multiplexing between channels using 32 internal priority levels • Priorities can be fixed or round-robin. • Major-minor loop structure. • $\overline{\text{DONE}}$ or $\overline{\text{DACK}}$ protocol.

Table 1. MSC7118 Features (Continued)

Feature	Description
Clocking, Interrupts, Control, and Debug	
Internal PLL	Generates up to 300 MHz clock for the SC1400 core and up to 150 MHz for the crossbar switch, DMA channels, M2 memory, and other peripherals.
Clock Synthesis Module	• Predivision on PLL input clock. • Independent clocking of the internal timers and DDR module. • Programmable operation in the SC1400 low power Stop mode. • Independent shutdown of different regions on the device.
Programmable Interrupt Controller (PIC)	Consolidates maskable interrupt and non-maskable interrupt sources.
System Control	• Software watchdog timer function. • Bus programmable time-out monitors on AHB-Lite slave buses. • Bus error detection and programmable time-out monitors on AHB-Lite master buses. • Address out-of-range and misaligned access detection on crossbar switch buses.
Programmable Address Detection	• Four user-programmable SC1400 core address detection units (program and data accesses). • Four user-programmable DMA address detection units. • Each detection unit supports: – Programmable range or value detection on the unit buses. – Optional generation of maskable/non-maskable interrupt on core detection units. – Optional generation of event trigger. – Status of detections captured in status register. • Programmable out-of-range detection, patching, or user-programmable error detection.
Event Port	• Collects important signals on the device: – EVNT pins – DMA request, start, and done signals. – Interrupt request signals.L • Signals are combined as programmed by the user to provide triggering to on-device units such as interrupts, breakpoints, DMA transfer requests, or wake-up from low-power stop mode. • Units can operate independently, can be sequenced, or can be enabled by an outside source. • Can be used independently or in conjunction with the OCE10 emulator debug port. • Output to EVNTx pins.
Boot	Booting from on-device peripherals: • Boot from HDI16 and I^2C. • Boot also from serial SPI Flash/EEPROM devices using software in the boot ROM to access SPI memory devices. • Different clocking options allow for boot operation with the PLL ON/OFF, as well as with different input frequency ranges.
Peripherals	
External Memory Interface	• DDR memory controller: – Byte enables for up to 32-bit external data bus. – Glueless interface to 150 MHz 14-bit page mode DDR-RAM. – 14-bit external address bus supporting up to 1 GB. – 16- or 32-bit external data bus. • Memory controller interface supports: – Programmable buffer significantly improves efficiency through DDR memory controller. – Independent read buffers. – Programmable predictive read feature for each read buffer. – Write buffer.

Table 1. MSC7118 Features (Continued)

Feature	Description
TDM Modules	Three independent TDM modules, each with the following features: • Totally independent receive and transmit, each having one data line, one clock line, and one frame sync line. • Frame sync line and/or clock line can be shared between receive and transmit within a single TDM or across all TDMs. • Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses. • Hardware A-law/μ-law conversion • Up to 50 Mbps per TDM (50 MHz bit clock). • Maximum rate is 1/4 the core frequency. • Up to 128 channels. • Each channel can be programmed to be active or inactive. • 8- or 16-bit word widths. • The TDM transmitter sync signal (TxTSYN) can be configured as either input or output. • The TDM transmitter clock signal (TxTCLK) can be configured as either input or output. • Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the frame sync signal and the beginning of the frame. • MSB or LSB first support.
Host Interface (HDI16)	Enhanced 16-bit wide interface provides a glueless connection to industry-standard microcomputers, microprocessors, and DSPs. The HDI16 can also operate with an 8-bit host data bus, making it fully compatible with the DSP56300 HDI08 from the external host side.
External Interfaces and Control Modules	External interfaces and control modules managed on the advanced peripheral bus (APB) including: • Three time-division multiplexing (TDM) modules, each supporting up to 128 channels. • Software watchdog timer. • 16-bit host interface (HDI16). • System control. • RS-232 interface/universal asynchronous receiver/transmitter (UART). • I^2C interface. • General-purpose input/output (GPIO) signals. • Interrupt controller to handle external interrupt functions (input and output). • Serial peripheral interface (SPI).
IPBus	Control modules on the IPBus include: • Programming model of the crossbar switch. • Programming model of the DMA controller. • Programming model of the DDR controller. • Clock synthesis module. • I^2C module. • System control unit. • Eight 16-bit timers.

Table 1. MSC7118 Features (Continued)

Feature	Description
Timers	Two identical quad timer modules, each with four 16-bit counter groups, have the following features: • Timers clocked from: – Primary and secondary clock inputs. – External event counting. – Cascadable operation. • Multiple counting modes: – Basic counting. – Dual-edge counting. – Gated count. – Quadrature count. – Signed up/down count. – Triggered count. • Capture and compare capability. • Broadcast mode. • Maximum rate is 1/4 the core frequency. • Tightly coupled with the event port. • Selectable interrupts: – Overflow. – Edge. – Compare, compare 1, compare 2.
UART	• Two signals for transmit data and receive data. • No clock, asynchronous mode. • Full-duplex operation. • Standard mark/space non-return-to-zero (NRZ) format. • 13-bit baud rate selection. • Programmable 8- or 9-bit data format. • Separately enabled transmitter and receiver. • Programmable transmitter output polarity. • Two receiver wake-up methods: – Idle line wake-up. – Address mark wake-up. • Separate receiver and transmitter interrupt requests. • Eight flags, the first five can generate interrupt request: – Transmitter empty. – Transmission complete. – Receiver full. – Idle receiver input. – Receiver overrun. – Noise error. – Framing error. – Parity error. • Receiver framing error detection. • Hardware parity checking. • 1/16 bit-time noise detection. • Maximum bit rate 5.0 Mbps. • Single-wire and loop operations.
I^2C Port	• 2-wire serial interface through GPIO. • Schmitt-trigger filtered inputs for noise suppression. • Compatibility with I^2C bus standard up to 100 kbps for standard mode and up to 400 kbps for Fast mode. • Bidirectional data transfer protocol. • Scalable clock rate of up to one MHz, starting at 50 kbps for the maximum core clock frequency. • Multiple-master operation that also allows any number of devices implementing the I^2C-master software module to access the memory simultaneously at boot or any time. • Compatible with the I^2C-serial EEPROM access protocol, allowing memory access of up to one MB.

Table 1. MSC7118 Features (Continued)

Feature	Description
General-Purpose I/O (GPIO) Port	Bidirectional signal lines that either serve the peripherals or act as programmable I/O ports. Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode. Port A lines can also be programmed as interrupt request inputs.
fieldBIST™ Hardware Diagnostics	Detects and provides visibility into unlikely field failures for systems with high availability. The Freescale unique fieldBIST ensures that the device: • Has structural integrity. • Operates at the rated speed. • Is free from reliability defects. Diagnostics can report partial or complete device inoperability. fieldBIST resolution can pinpoint the following uniquely: • 6 memory blocks, including ROM. • 3 logic levels (top, extended core, and peripherals). • 1 PLL. Simple JTAG interface allows easy integration to system firmware.
Reduced Power Dissipation	• Very low power CMOS design. • Separate power supply for internal logic and I/O. • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
Packaging	• 400-ball MAP-BGA. • 17 × 17 mm. • 0.8 mm pitch. • Pb-free or Pb-bearing packaging technology.
Software and Hardware Support	
Software Support	Real-time operating systems (RTOS) that fully supports MSC7118 device architecture (multi-core, memory hierarchy, ICache, timers, DMA, interrupts, peripherals). This operating system, called SmartDSP OS, is bundled with CodeWarrior™: • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs. • Fully supports MSC7118 DMA, interrupts, and timer schemes. Distributed system support, enables transparent inter-task communications: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Includes integrated device drivers for such peripherals as TDM, UART, and external buses.
	Additional features: • Incorporates task debugging utilities integrated with compilers and vendors. • Board support package (BSP) for MSC711xADS.
	CodeWarrior Integrated Development Environment (IDE): • C/C++ compiler with in-line assembly. Enables the developer to generate highly optimized DSP code. It translates code written in C/C++ into parallel fetch sets and maintains high code density. • Librarian. Enables the user to create libraries for modularity. • C libraries. A collection of C/C++ functions for the developer's use. • Linker. Highly efficient linker to produce executables from object code. • Debugger. Seamlessly integrated real-time, non-intrusive multi-mode debugger that enables debugging of highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. • Profiler. An analysis tool using a patented Binary Code Instrumentation (BCI) technique that enables the developer to identify program design inefficiencies.

Table 1. MSC7118 Features (Continued)

Feature	Description
Application Development System (ADS) Board	• Host debug through a single JTAG connector supports both the host processor and the MSC7118 device. • Two kinds of ADS configurations: one with a host CPU and one without a host CPU. • Big Flash memory for stand-alone applications. • Support for the following communications ports: – 10/100BaseT. – T1/E1 TDM interface. – H.110. – Voice codec. – RS-232. – High-density (MICTOR) logic analyzer connectors to monitor MSC7118 signals. – 6U cPCI form factor. • Emulates DSP farm by connecting to three other ADS boards.
Low-Cost General-Purpose EVM Board	• 32 MB of DDR SDRAM memory. • 16-bit audio codec (3.5 mm jacks). • 256 KB I^2C EEPROM. • TDM interface. • Host port interface. • JTAG interface. • RS-232 interface.

Product Documentation

The documents listed in **Table 2** are required for a complete description of the MSC7118 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP web site. See the contact information on the back cover of this document.

Table 2. MSC7118 Documentation

Name	Description	Order Number
MSC7118 Technical Data	MSC7118 features list and physical, electrical, timing, and package specifications	MSC7118
MSC7118 Reference Manual	Detailed functional description of memory and peripheral configuration, operation, and register programming	MSC7118RM
SC1000 Family Processor Core Reference Manual	Detailed description of the SC1000 family processor cores, including the SC1400, and instruction set	10180-01 See the StarCore LLC web site at www.starcore-dsp.com
OCE10 On-Chip Emulator Reference Manual	Information on the architecture and programming model of the OCE10 on-chip emulator, which is the StarCore implementation of the EOnCE™. The OCE10 on-chip emulator is a peripheral that facilitates debugging the StarCore SC1000-family processor core and peripherals.	10055-03
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC7118 product web site

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