MMC2075

MMC2075 32-Bit Microcontroller Product Brief

The MMC2075 is designed to provide the marketplace with a powerful and flexible solution for designs in the new millennium. The MMC2075 integrates one of Motorola's most successful product families— M•CORE™—with essential peripherals, providing designers with a combination that sets a new performance standard while requiring less power. The component parts of the MMC2075 are shown in Figure 1 on page 2.

The MMC2075 is a member of the low-power, high-performance M•CORE family of 32-bit microcontroller units (MCUs). It contains an M•CORE CPU, a streamlined execution engine that provides many of the performance enhancements found in mainstream reduced instruction set computers (RISCs). Combining performance, speed, and cost efficiency in a compact, low-power design, the M•CORE microRISC architecture is a natural solution for applications where battery life and systems cost are critical design goals.

The MMC2075 reduces power consumption by coupling a fully static design with dynamic power management and low-voltage operation. Versatile power management is achieved through automatic power downs of any internal functional blocks that are not needed on a clock-by-clock basis. Power conservation modes are also provided for absolute power conservation.
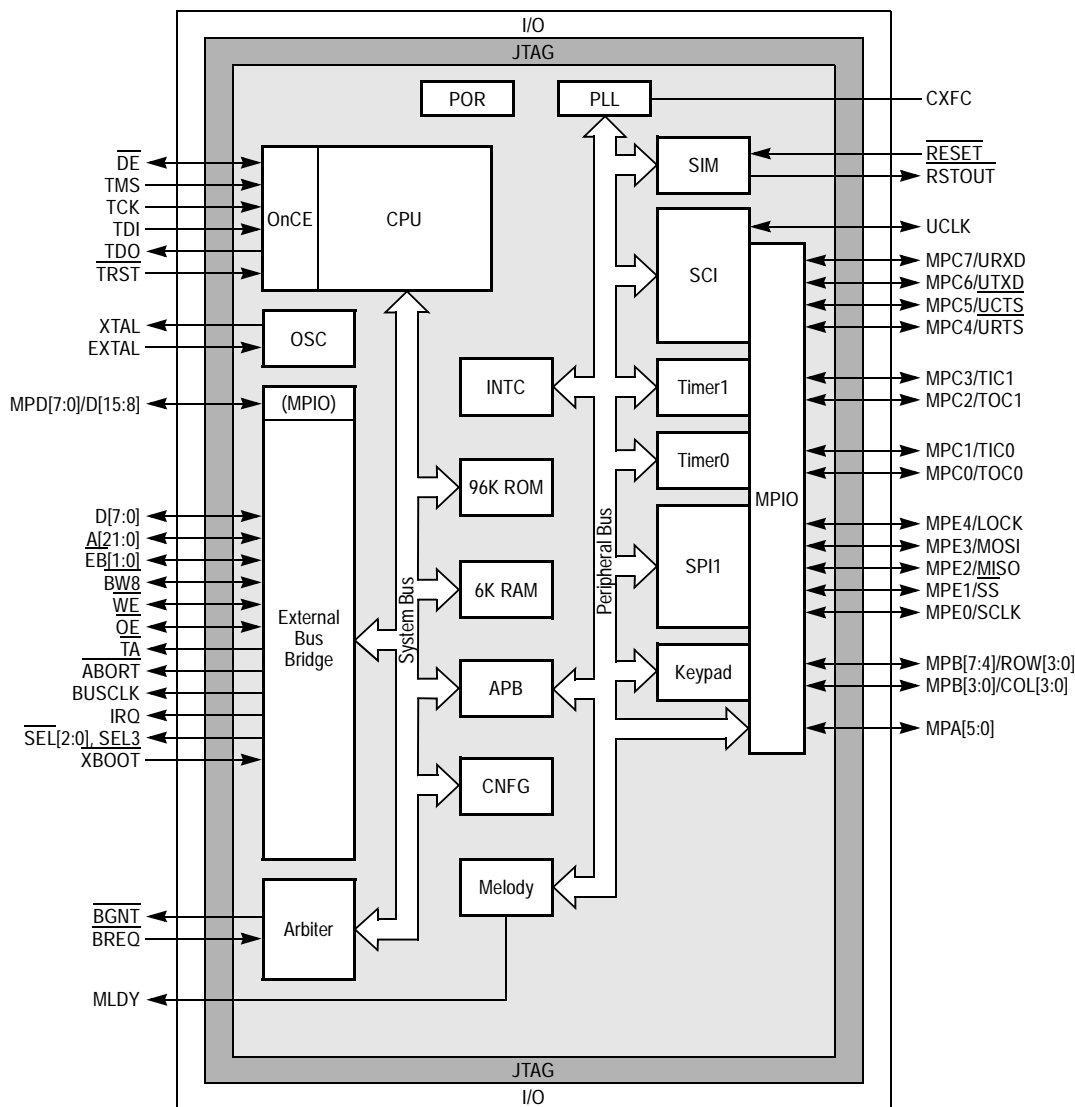
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Figure 1. MMC2075 (144-Pin) Block Diagram

1.1 Key Features

The key features of the MMC2075 are as follows:

- • M•CORE RISC Processor
  - — 32-bit load/store M•CORE RISC architecture
  - — Fixed 16-bit instruction length
  - — 16-entry 32-bit general-purpose register file
  - — 32-bit internal address and data buses
  - — Efficient four-stage, fully interlocked execution pipeline
  - — Single-cycle execution for most instructions; two cycles for branches and memory accesses
  - — Special branch, byte, and bit-manipulation instructions

- — Support for byte, halfword, and word memory accesses
- — Fast interrupt support via vectoring/auto-vectoring and a 16-entry dedicated alternate register file
- On-chip memory
  - — 24K × 32 CPU ROM (96K)
  - — 1.5K × 32 CPU RAM (6K)
- On-chip peripherals
  - — Asynchronous serial communications interface (SCI) with IrDA capability
  - — Synchronous serial peripheral interface (SPI)
  - — Melody generator
  - — 4 × 4 keypad interface
  - — Multipurpose I/O ports (MPIO)
  - — Two 16-bit general purpose timers
  - — Time-of-day (TOD) timer
  - — Watchdog timer
  - — Vectored interrupt controller with 16 programmable priority levels
  - — Oscillator and PLL with software-selectable speeds
  - — AMBA peripheral bridge that depipelines system bus for simpler peripheral bus
  - — 8/16-bit external system bus with 22-bit address bus
- Operating features
  - — Processor operation to 10 MHz over full operating range
  - — Low-power modes
  - — OnCE™ debug module
  - — Voltage range 1.8 V to 3.6 V; temperature range –20 °C to 85 °C
  - — Chip select outputs for four external devices (4 Mbyte per chip select, 16 Mbyte directly addressable)
  - — Programmable wait states for external accesses
  - — External boot option

1.2 Suggested Reading

The following documents are required for a complete description of the MMC2075 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola Semiconductor Products Sector sales office, a Motorola Literature Distribution Center, or the World Wide Web.

M•CORE Reference Manual (order number MCORERM/D)

MMC2080/2075 Advance Information (order number MMC2080/2075/D)

MMC2080/2075 32-Bit MCU User's Manual (order number MMC2080UM/D)

1.3 Additional Information

Additional information on the M•CORE architecture and development tools can be found at the Web site http://www.motorola.com/mcore.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado, 80217
1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan, Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku,
Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd., Silicon Harbour Centre, 2 Dai King Street,
Tai Po Industrial Estate, 2 Tai Po, N.T., Hong Kong. 852-26668334

Customer Focus Center: 1-800-521-6274

Mfax™: RMFAX0@email.sps.mot.com   –TOUCHTONE 1-602-244-6609
–US & Canada ONLY 1-800-774-184
–http://sps.motorola.com/mfax/

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