DSP56007ROM
DSP56L007ROM

Product Brief
24-bit Digital Signal Processor

The DSP56007 and the low-voltage DSP56L007 are high-performance, programmable Digital Signal Processors (DSPs) suitable for a variety of digital audio decompression functions needing more memory, such as Dolby AC-3, MPEG Layer 2, and ATRAC. The DSP56007/L007 is an MPU-style general purpose DSP, composed of an efficient 24-bit digital signal processor core, large program and data memories, various peripherals optimized for audio, and support circuitry. As illustrated in Figure 1, the 56000-Family-compatible DSP core is fed by a large program ROM, two independent data RAMs, and two data ROMs, a Serial Audio Interface, Serial Host Interface, External Memory Interface, dedicated I/O lines, on-chip Phase-Locked Loop (PLL), and On-Chip Emulation (OnCE™) port.

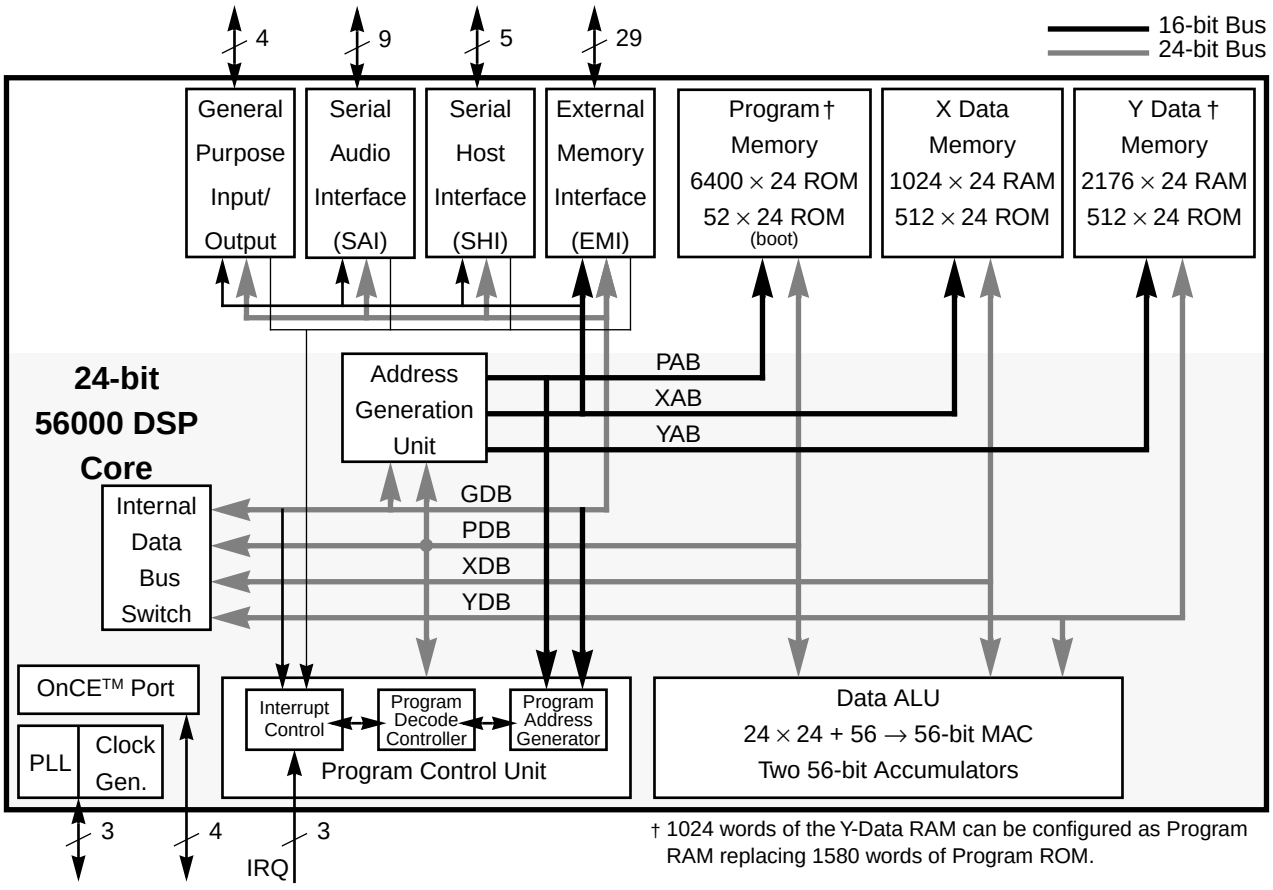

Figure 1 DSP56007/L007 Block Diagram

Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

DSP56007/L007 Features

Digital Signal Processing Core

- Efficient, object code compatible, 24-bit 56000-Family DSP engine
  - —Up to 33 Million Instructions Per Second (MIPS) – 30.3 ns instruction cycle at 66 MHz
  - —Up to 180 Million Operations Per Second (MOPS) at 66 MHz
  - —Highly parallel instruction set with unique DSP addressing modes
  - —Two 56-bit accumulators including extension byte
  - —Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - —Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
  - —56-bit addition/subtraction in 1 instruction cycle
  - —Fractional and integer arithmetic with support for multiprecision arithmetic
  - —Hardware support for block-floating point Fast Fourier Transforms (FFT)
  - —Hardware nested DO loops
  - —Zero-overhead fast interrupts (2 instruction cycles)
  - —Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories

Memory

Table 1 lists the memory configurations of the DSP56007/L007.

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 6400 × 24-bit on-chip program ROM* and 52 × 24-bit bootstrap ROM
- 1024 × 24-bit on-chip X-data RAM plus 512 × 24-bit on-chip X-data ROM*
- 2176 × 24-bit on-chip Y-data RAM plus 512 × 24-bit on-chip Y-data ROM*
- 1024 × 24 bits of the Y-data RAM can be configured as program RAM, replacing 1280 × 24 bits of program ROM
- Bootstrap loading from Serial Host Interface or External Memory Interface
- Proprietary Bootstrap for Securing Program ROM contents

Table 1 DSP56007/L007 Memory Configurations

Mode	Program		X Data		Y Data	
	ROM	RAM	ROM	RAM	ROM	RAM
Mode 1	6400*	none	512*	1024	512*	2176
Mode 2	5120*	1024	512*	1024	512*	1152

Word width is 24 bits.

* These ROMs may be factory-programmed with data/program provided by the application developer.

Peripheral and Support Circuits

- Serial Audio Interface (SAI) includes 2 receivers and 3 transmitters, master or slave capability, and implementation of I^2S, Sony, and Matshushita audio protocols; two sets of SAI interrupt vectors
- Serial Host Interface (SHI) features single master capability, 10-word receive FIFO, and support for 8-, 16- and 24-bit words
- External Memory Interface (EMI), implemented as a peripheral supporting:
  —Page-mode DRAMs (one or two chips): 64k × 4, 256k × 4, and 4M × 4 bits
  —SRAMs (one to four): 256k × 8 bits
  —Data bus may be 4 or 8 bits wide
  —Data words may be 8, 12, 16, 20, or 24 bits wide
- Four dedicated, independent, programmable General Purpose I/O (GPIO) lines
- On-chip peripheral registers memory mapped in data memory space
- Three external interrupt request pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based (PLL) frequency synthesizer for the core clock
- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 40, 50, and 66 MHz down to DC (DSP56L007 operates only up to 40 MHz)
- 80-pin plastic Quad Flat Pack surface-mount package; 14 × 14 × 2.45 mm; 0.65 mm lead pitch
- Completely pin compatible with the DSP56004 for easy upgrades
- 3.3 V (DSP56L007) and 5 V (DSP56007) power supply options

The DSP56007 and DSP56L007 are identical except that the DSP56007 operates at 5 volts and up to 66 MHz, while the DSP56L007 operates at 3.3 volts and up to 40 MHz with a resultant reduction in power consumption and the need for fewer batteries in a portable application. The DSP56007/L007 is a pin-compatible version of the DSP56004 with a different memory configuration.

Documentation

The three documents listed in Table 2 are required for a complete description of the DSP56007/L007 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center listed below.

Table 2 Additional DSP56007/L007 Documentation

Document Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56004/007 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56004UM/AD
DSP56004/007 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56004/D

Literature Distribution Centers
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona USA 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbor Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.