New QorIQ Generation: AMP Up Your Performance

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Introduction

Freescale has been meeting the needs of thousands of customers with generations of PowerQUICC and QorIQ communications processors. As market conditions evolve, it has proved challenging to deliver the horsepower, lower power and easier-to-use tools that customers require with standard silicon manufacturing techniques. As a result of this, Freescale recently announced the next generation QorIQ Advanced Multiprocessing (AMP) series of processors, built on 28 nm process technology, which redefines levels of performance and power efficiency not previously attainable.

Challenges Faced by Equipment Vendors

Moore's Law states that the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years. Today's network bandwidth challenges Moore's Law—traffic is doubling every 12 months as the demand for social media and rich content grow. The insatiable demand for connectivity will continue to push the industry for solutions that deliver performance beyond Moore's Law, with improved efficiency and lower operating costs.

Freescale Power Architecture® Solutions

Freescale QorIQ communications platforms provide developers with a series of multicore processors based on high-performance Power Architecture® cores. These processors meet the through-put requirements for today's infrastructure applications that need robust real-time, point-to-point communication. QorIQ processors provide an evolutionary step up that preserves legacy investments in earlier generation PowerQUICC communications processors. The workhorse of the QorIQ P series is the P4080 processor with eight integrated e500mc cores, operating at frequencies up to 1.5 GHz, combined with high-

Figure 1: New Advanced Multi-Threaded e6500 Core

Improvement of DMIPs Per Thread	Dual Thread Efficiency	Frequency	Number of Cores
	2.4x	1.3x	1.5x
IPC Improvements	**Multi-threading**	**Frequency Improvements**	**Multicore**
• 64-bit architecture • AltiVec Technology: 240 GFLOPS • 1TB physical address • Accelerate Hypervisor performance with LRAT	• Dual thread • Each with separate front end, branch unit and LSU • Larger amount of onboard cache per core	• New process and e6500 core allowing increased frequency	• Up to 24 virtual cores • Large 2 MB shared L2 cache within a cluster of one to four cores • CoreNet cache-coherent fabric with multiple clusters to scale from one to eight clusters • Virtualization

>4x performance improvement over previous generation

performance data path acceleration (DPAA) logic, and network and peripheral bus interfaces in a 45 nm implementation. Freescale's QorIQ AMP series is able to push its compute and energy performance envelope beyond the P4080 processor (Figure 1) such that its performance capacity exceeds that which Moore's Law predicts.

By taking advantage of multiple innovations that work together, QorIQ AMP series processors are able to improve software developer productivity while delivering a better than 4x improvement in application and core processing performance, and also deliver a better than 2x improvement in power efficiency (over the P4080 device). Key innovations that enable these improvements include advanced multi-threaded e6500 core, improvements in the high-performance memory, interconnects and application-specific accelerators, all implemented in a 28 nm process.

Energy efficiency is improved by better than 2x over the previous generation QorIQ devices through advanced power management such as the inclusion of cascading power management for core and system power management, special attention to multicore clustering optimizations and aggressive use of hardware acceleration.

e6500 Core

The advanced multi-threaded e6500 core is based on a 64-bit architecture sporting large L1 caches and a 2x 2-way superscalar execution engine that can operate at up to 2 GHz, which is a 1.3x frequency improvement over the e500mc in the P4080.

Register settings allow developers to use 32-bit or 64-bit mode. A hybrid 32-bit mode supports e500 legacy software and supports a smooth transition to the 64-bit architecture. The e6500 core provides a dual-thread capability that enables each core to act as two virtual cores. Each thread has dedicated fetch, decode, issue and completion resources. Each thread also has a dedicated branch unit, load/store unit (LSU) and simple fixed point execution units. The complex fixed point execution unit as well as the floating point unit and the AltiVec vector engine are shared between threads.

Each e6500 core is able to address up to 1 TB of memory space. The first product scheduled to be released in the QorIQ AMP series is the T4240 processor. This processor has 12 dual-threaded cores (24 virtual cores) where each dual-threaded e6500 core can be clustered in groups of four cores that share a common 2 MB L2 cache. The CoreNet cache-coherent fabric scales to support up to eight multiple clusters in a single system.

Optimizations in the memory architecture yield 2.4x improvement in the memory bandwidth and 1.6x improvement for the double data rate (DDR) clock frequency over previous generation QorIQ processors.

The e6500 core includes several features to support hardware-assisted virtualization, such as an extra privilege level for hypervisor support. Hardware support for logical to real address translation (LRAT) considerably reduces hypervisor overhead. A new logical partition ID field enables developers to identify partitions for virtual to real address translation. I/O MMU-like capabilities were added to the system to prevent data corruption for DMA or I/O. Network-bound interfaces are virtualized, and virtualization of hardware blocks is supported via the QMan for best-effort virtualization.

The e6500 core includes a 16 GFLOPS AltiVec execution unit that is able to improve the performance of algorithms such as the scheduler algorithm and media processing by a factor of four over a C-optimized implementation on the P4080. AltiVec technology is a vector or single instruction multiple data (SIMD) architecture that allows the simultaneous processing of multiple data items in parallel.

The QorIQ AMP series includes additional application-specific accelerators such as a security engine (SEC), DPAA, data flow acceleration, pattern matching engine (PME) and a hardware decompress/compress engine (DCE) that can dramatically improve network processing.

The QorIQ AMP processors push beyond a 2x improvement in power efficiency over previous generation QorIQ devices. Implementing the AMP processors in a 28 nm process yields 50 percent power savings. The cascading power management architecture enables reduced energy consumption under light network loads and automatically returns to full function when network loads increase. Developers are also able to dynamically set and change core operating frequencies for each cluster of cores.

The cascading power management architecture supports a state retention power gating (SRPG) "fast on, fast off" technique that allows the voltage supply to be reduced to zero for the majority of a block's logic gates while maintaining the supply for the state elements of that block to support fast wake up times. Because these processors do not have to save/restore processor state to memory, they have a greater than 10x improvement in their wake up response time.

QorIQ AMP processors build on the architecture powering existing QorIQ processors, and they maintain software code compatibility with the existing QorIQ P series, QorIQ Qonverge and PowerQUICC processors. On-chip, in-silicon debugging support includes deep inspection debug that provides visibility at the core, accelerator and fabric level of the processor. Full system trace includes change of flow, process and originator trace that is integrated with instrumented OS trace. A developer has complete control of event configuration to best be able to monitor, trigger, timestamp and count thousands of core/SoC events and user-defined messages. The debug architecture enables tracking core interactions with advanced cross-triggering. Built-in security mechanisms prevent debug interface intrusions. The debugging system also supports configurable black box recording for post-mortem debug. Development is supported by Freescale's CodeWarrior tools and VortiQa software, as well as third-party tools from Enea®, Green Hills®, Mentor Graphics, QNX® and Wind River®.

QorIQ T4240 Processor

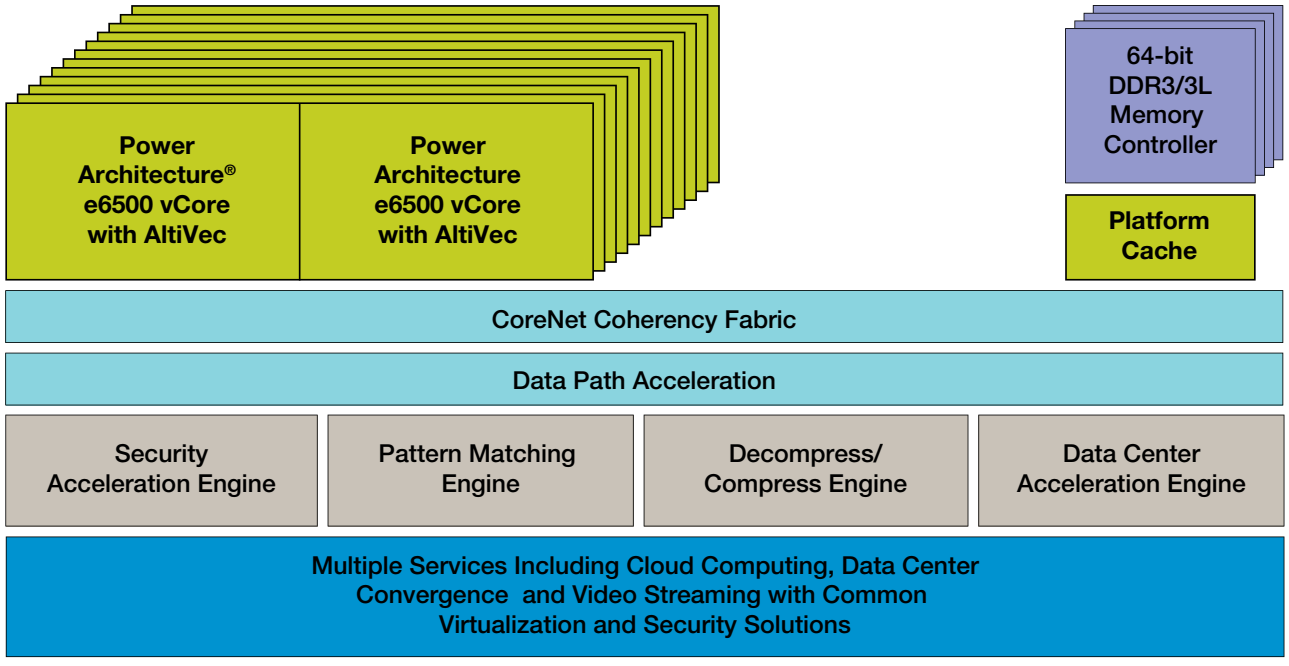
The QorIQ T4240 (Figure 2) is the first AMP series device scheduled for release in 2012 and targets data center networking, metro carrier edge/core routers, aerospace and defense, as well as access gateway applications. Additional AMP devices are planned for release each quarter thereafter. The T4240 processor integrates twelve e6500 cores in a single device that are organized into three processor clusters of four cores each. The 24 virtual cores are able to operate at up to 1.8 GHz and support processing for 48 Gbps packet throughput.

System performance for the QorIQ AMP T4240 processor is rated at up to 4x better than the CPU performance of the previous generation eight-core P4080 device. The L2 cache is six times larger. The T4240 processor delivers 3x better acceleration for data path acceleration and 2x better throughput for the CoreNet fabric, security engine, OCEAN and data flow acceleration blocks. New functions of data decompression/compression accelerator (20 Gb per second), Interlaken Look-Aside (80 Gb per second), PCIe 3.0, SR-IOV end point and data center bridging are not available on the P4080 and are new with the T4240 processor.

Conclusion

Smaller process implementations demonstrate that technology scaling continues to deliver benefits. At 28 nm, QorIQ processors experience 50 percent lower power to retain constant processing performance while enjoying a 40 percent silicon area reduction over 45 nm implementations. Freescale's experience with 28 nm process technology continues to suggest that next-generation application performance will be achieved through a combination of smaller process nodes and the use of more processing engines—in the form of more cores and accelerators. This combination is expected to deliver up to 4x improvement in application performance at the new process node, exceeding the limitation of Moore's Law and helping to enable a more connected world.

Figure 2: QorIQ T4240 Proposed Structure



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