

Heat sink small outline package (HSOP) and power quad flat package (PQFP) PCB assembly guidelines

1 Introduction

This application note provides guidelines for the handling and assembly of NXP'S heat sink small outline package (HSOP) and power quad flat package (PQFP) during printed circuit board (PCB) assembly.

Guidelines for PCB design, rework, and package performance information, such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data are included for reference.

2 Scope

This document contains generic information encompassing various NXP HSOP and PQFP packages assembled internally or at external subcontractors.

Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.nxp.com, or contact the appropriate product application team.

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3 HSOP and PQFP package information

Figure 1 shows the standard HSOP and PQFP offerings through NXP.

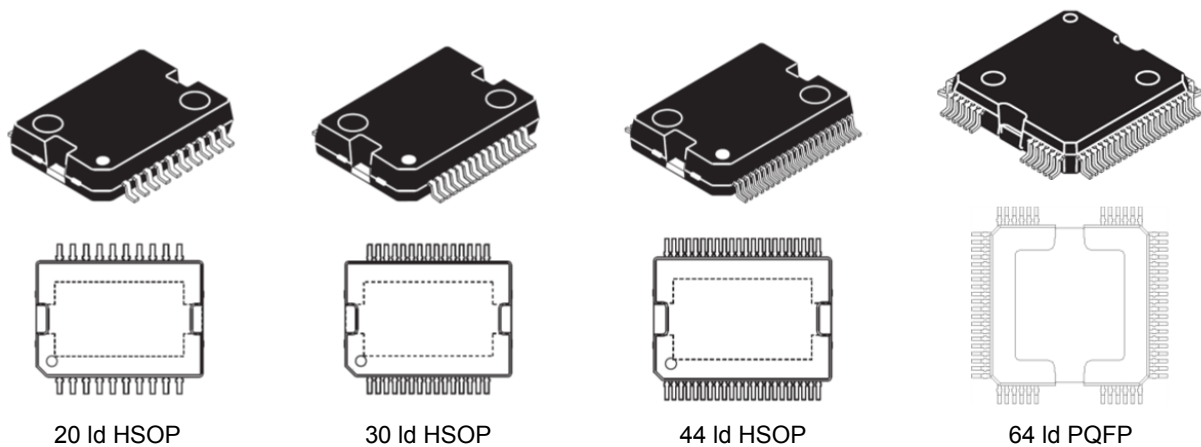


Figure 1. Standard NXP HSOP and PQFP offerings

3.1 Package description

The HSOP and PQFP are surface mount integrated circuit packages. The standard form is a flat rectangular or square body, with leads extending from two or four sides. This package has a mechanically attached thick Copper (Cu) heat sink to improve the thermal performance. The exposed heat sink provides a direct path for heat conduction away from an IC and into a solder attached printed circuit board (PCB). The leads are formed in a gull wing shape to allow solid footing during assembly to a PCB. Standard Pb-free lead finish on HSOP packages is NiPdAu and on PQFP packages is matte Sn.

3.2 Package dimensions

HSOP and PQFP packages are offered in industry standard body sizes with different lead counts and pitches. See Figure 1. Refer to NXP package case outline drawings to obtain detailed dimensions and tolerances. NXP's HSOP package is a non-JEDEC package, while PQFP is JEDEC MO-188. The HSOP exposed pad region was widened to improve thermal performance compared to the JEDEC MO-166 package (See reference [17]). Check with the NXP sales team for more information.

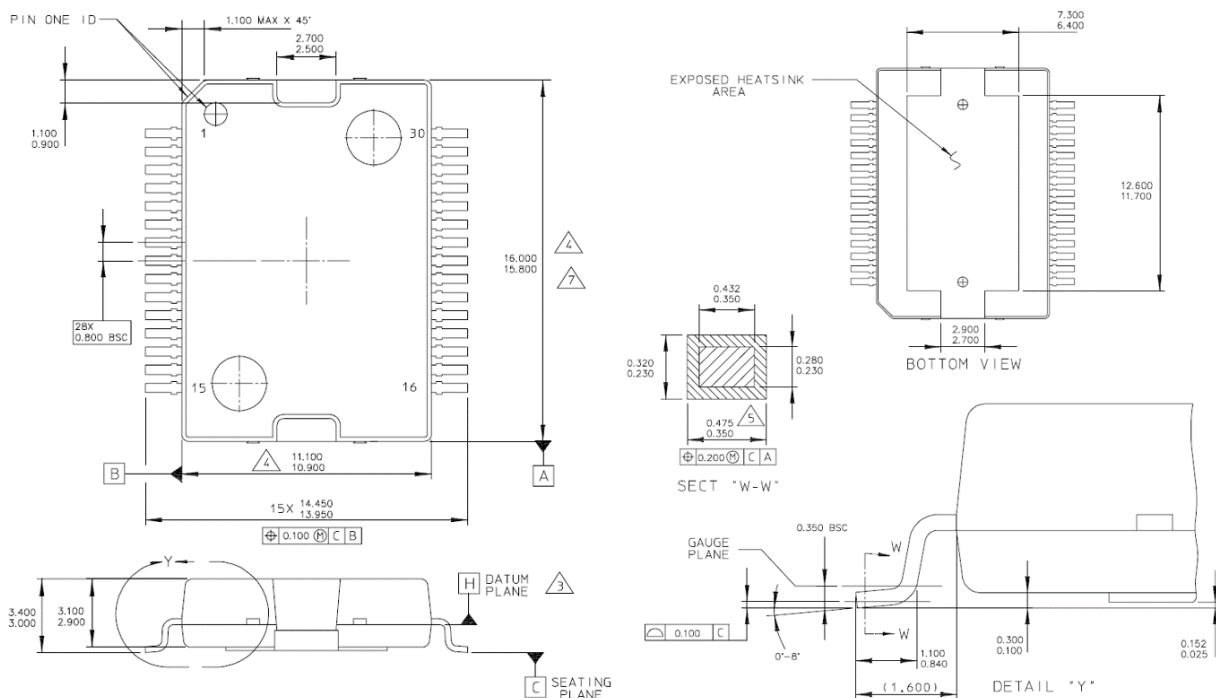


Figure 2. Example of a HSOP 30 LD case outline drawing

Table 1. Standard NXP HSOP and PQFP offerings

Package	I / O	Package body size width (in.)	Package body size length (in.)	Package height max. (in.)	Package pitch
HSOP 20	20	11.0	15.9	3.2	1.27
HSOP 30	30	11.0	15.9	3.2	0.80
HSOP 44	44	11.0	15.9	3.2	0.65
PQFP 64	64	14.0	14.0	3.15	0.65

3.3 Package cross-section

The cross-section drawing in Figure 3 shows a typical HSOP configuration. Pre-plated Cu lead frame and a thick Cu heat sink are mechanically riveted. Solder die attach and Cu wire are used for standard die attach and bond wire material, and encapsulated with epoxy mold compound.

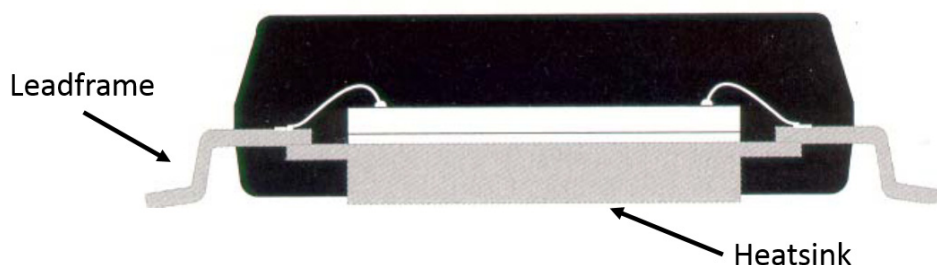


Figure 3. Cross-section of an HSOP package

4 Printed circuit board guidelines

4.1 PCB design guidelines and requirement

Proper PCB footprint and stencil designs are critical to ensure high surface mount assembly yields, and electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package case outline drawings are available at www.nxp.com. Follow the procedures in [Section 9.1 Case outline drawing, MCDS and MSL information download, page 20](#). [Figure 2](#) shows an example of an HSOP 30-lead case outline drawing. The goal is a well soldered HSOP gull wing lead as shown in [Figure 4](#).

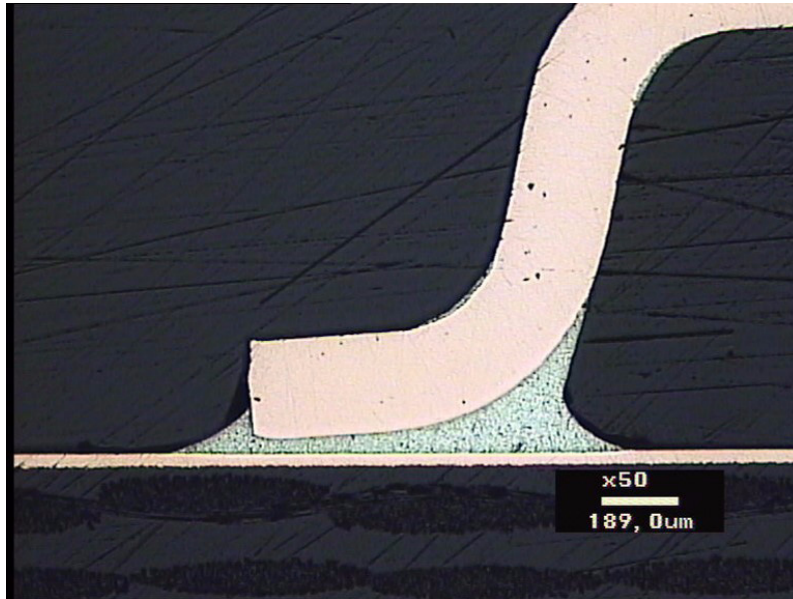


Figure 4. 50x magnified optical microscope image of a well soldered HSOP lead based on a robust pad design

4.2 PCB pad design

NXP follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the IPC's web site (landpatterns.ipc.org/default.asp) and includes guidelines for HSOP based on assumed package dimensions.

4.2.1 General pad guidelines

Some general guidelines for HSOP footprints are:

- Lead foot should be approximately centered on the pad with equal pad extension from the toe and the foot.
- Typically, the pad extends 0.5 mm beyond the HSOP foot at both the heel and the toe.
- Care should be taken so PCB pads do not extend under the HSOP body, which can cause issues in assembly.
- Pad width should be approximately 60% of the lead pitch - See [Table 2](#)
- Pitch needs to be designed in metric using the exact dimensions of 0.65 mm and 1.27 mm.

Table 2. Suggested PCB pad widths as a function of lead pitch ⁽¹⁾

Lead pitch (mm)	Pad width (mm)
0.65	0.45
0.80	0.60
1.27	0.65

Notes

1. Some legacy products may have alternate pitches.

Using the example of the 30-lead HSOP in Figure 2, the PCB pad width should be designed at 0.60 mm (X1) for this 0.80 mm lead pitch package. To determine the placement and length of the pads, obtain the tip to tip dimension from the package drawing (Figure 2). It has a range of 13.95 mm to 14.45 mm or a nominal dimension of 14.20 mm. Similarly, the foot length has a range of 0.84 mm to 1.10 mm with a nominal of 0.95 mm. The pad should be 1.95 mm (Y1) in length which is the 0.95 mm nominal foot length with a 0.50 mm extension on the heel and toe sides. Land center to center (C) is 13.20 mm, package nominal tip to tip dimension of 10.30 reduced by half of the foot length 0.35 mm on both sides. See Figure 5. Refer to Table 3 for Heat sink tab dimensions. These dimensions remain the same for other HSOPs.

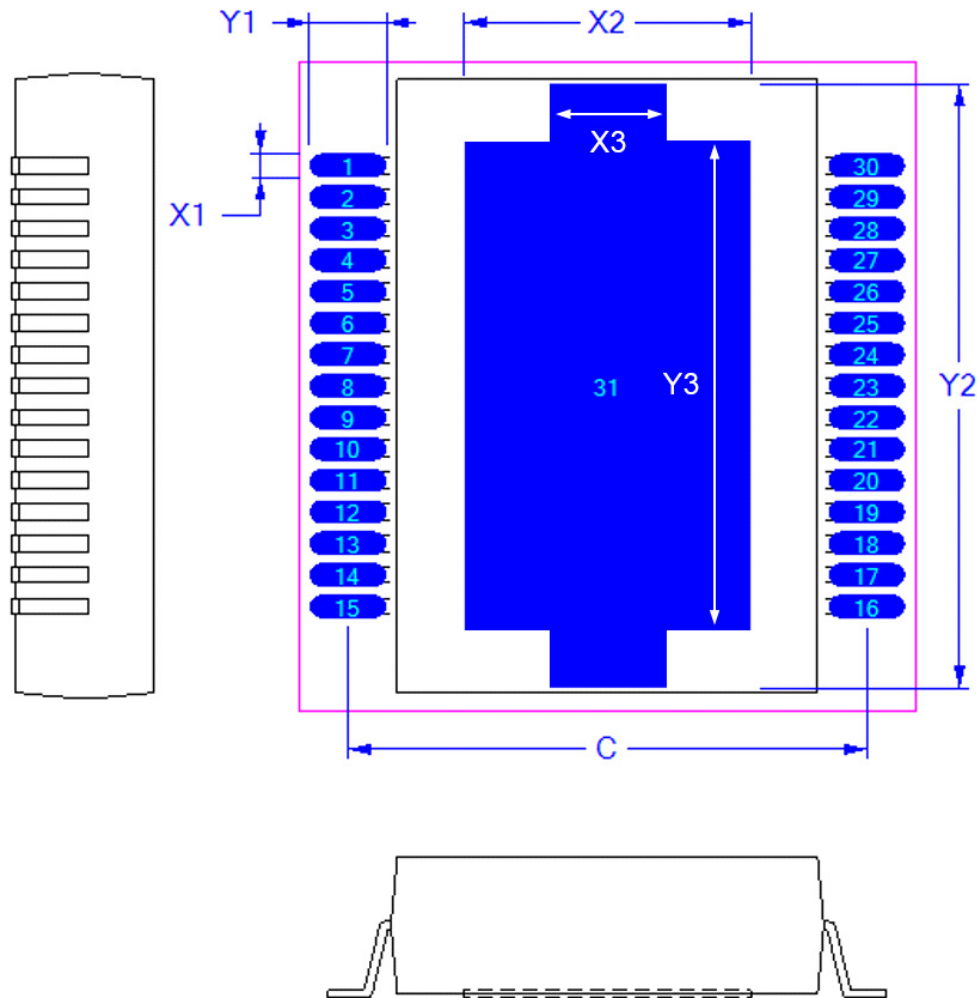


Figure 5. Typical HSOP land pattern

Table 3. HSOP land pattern dimension

Symbol	Typical dimension (mm)
C	13.2
X1	0.6
Y1	1.95
X2	7.1
Y2	15.85
X3	2.8
Y3	12.35

4.2.2 Thermal/electrical pad guidelines

Exposed pad (EP) HSOP packages are based on a thermally/electrically enhanced lead frame technology. The bottom of the package provides the primary heat removal path, as well as excellent electrical grounding to the PCB. In an EP package, the die attach paddle is down-set within the package such that the pad is exposed during the mold process. In [Figure 6](#), white arrows show the heat flow. To optimize thermal performance, the PCB design should include a thermal plane as shown in [Figure 6](#).

Although the land pattern design for EP lead attachment on the PCB should be the same as that for conventional, non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled packages may involve extra steps, depending upon the current rework practice within the company.

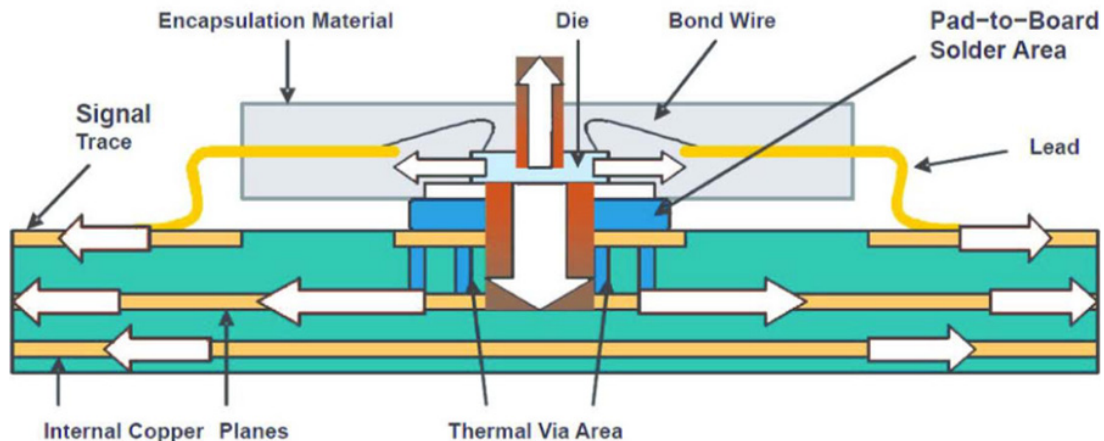
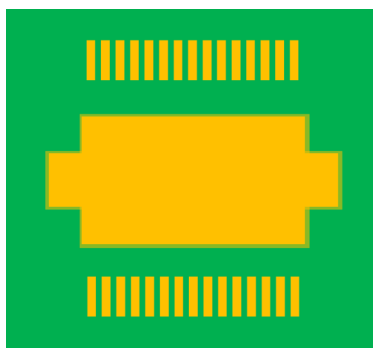


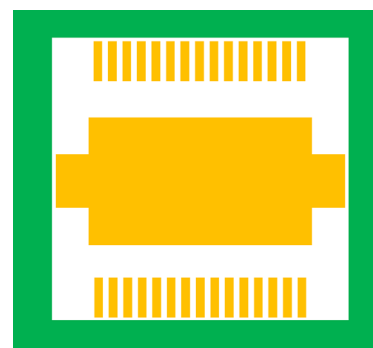
Figure 6. Cross-section of an HSOP package with heat transfer schematic

4.2.3 Spacing between PCB pads for leads and exposed pad

In order to maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 7](#). The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the land pattern and the inner edges of leads pad pattern to avoid any shorts. This topic is discussed in more detail in [Section 5.2 Solder stencil/solder paste](#), page 10.



SMD exposed pad land pattern



NSMD exposed pad land pattern

Figure 7. Example of exposed pad land pattern

4.2.3.1 Alternative exposed pad design

The exposed pad solder land can be segmented into a pad array as shown in [Figure 8](#). The pad array should be created by segmentation of a full copper area by solder mask webbing. Recommended edge length of a matrix pad is between 1.0 mm to 2.0 mm, the distance between the individual pads should be 0.2 mm to 0.4 mm. The minimum distance (width of the solder mask webbing) needs to be aligned with the PCB manufacturers design rules and manufacturing capabilities.

The segmented PCB design facilitates the solder paste flux out gassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

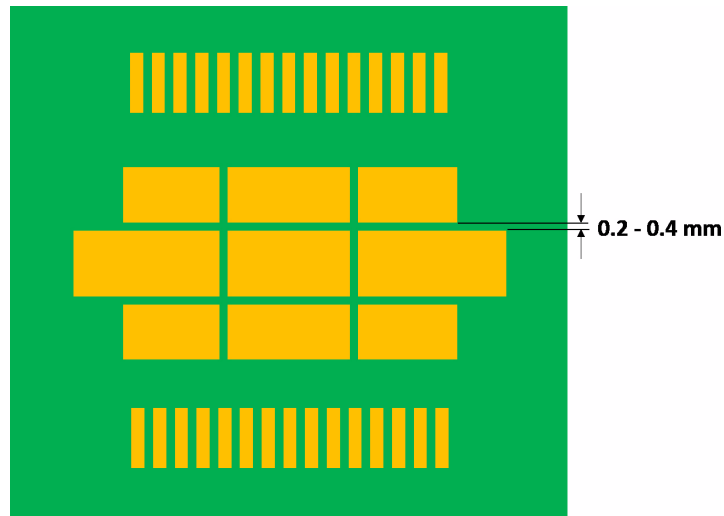


Figure 8. PCB exposed pad land pattern segmented by solder mask

Alternatively, the exposed pad solder land can be segmented into a symmetric pad array as shown in [Figure 9](#). The pad array can be created either by segmentation of a full copper area by solder mask, or copper defined outlines using NSMD pads. Recommended edge length of a matrix pad is between 1.0 mm to 2.0 mm, the distance between the pads should be 0.4 mm.

The segmented PCB design facilitates the solder paste flux out gassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

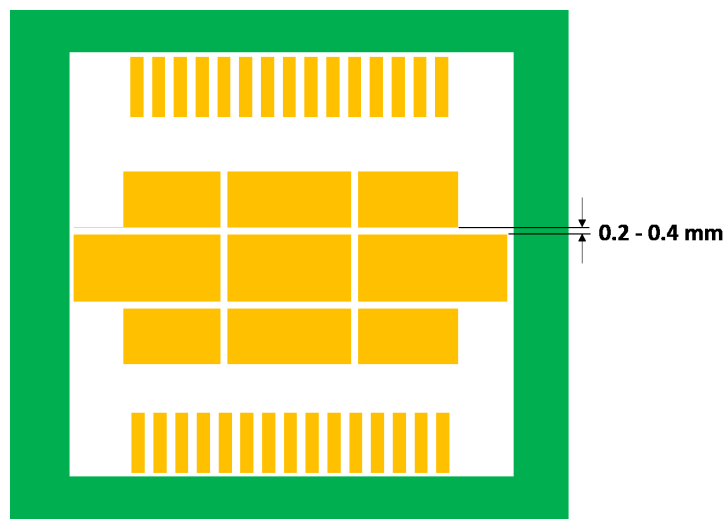


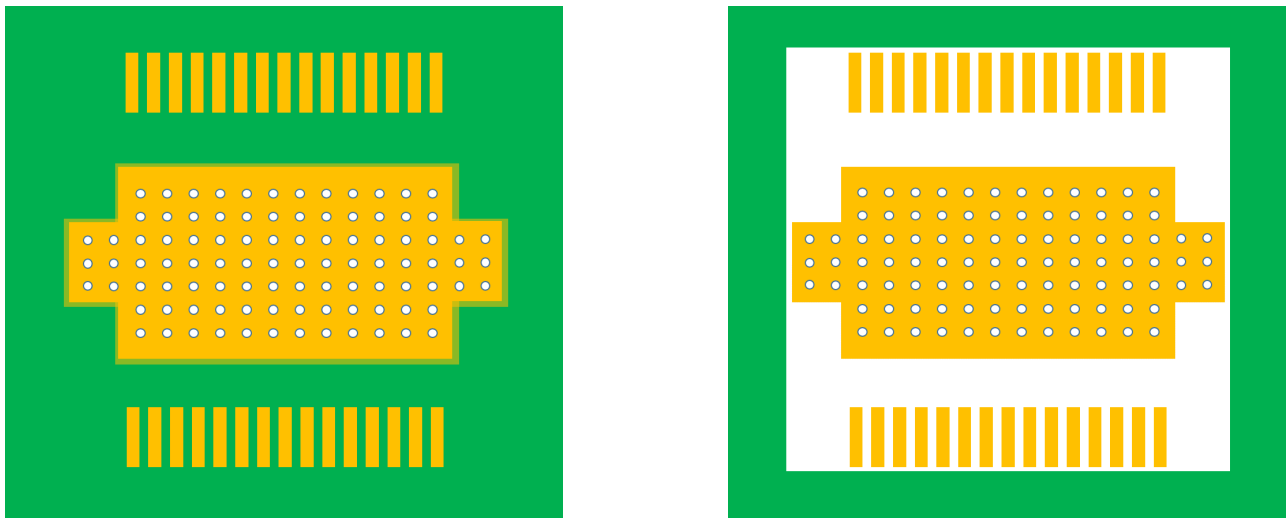
Figure 9. PCB exposed pad land pattern segmented by copper defined pads

4.2.4 Vias in the PCB EP pads

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct heat from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number required. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 1.2 mm grid pitch, as shown in [Figure 10](#).

It is also recommended that the via diameter should be 0.30 mm to 0.33 mm with 1.0 oz. copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

Note: These recommendations are to be used as a guideline only.



0.3 mm Ø at 1.2 mm Pitch Thermal Via

Figure 10. PCB exposed pad via grid

4.2.4.1 Vias in alternative exposed pads

For solder mask defined array pad design option, there are various thermal via arrangements possible.

- Via is placed in the center of the pad, as show in [Figure 11](#) (left image).
- Vias can be placed in the cross-points of the solder mask webbing.

For copper defined array pad design option, it is recommended to place the thermal via in the center of the pad, as show in [Figure 11](#) (right image). All the vias in these two pad design options must be plugged, tented, or plated.

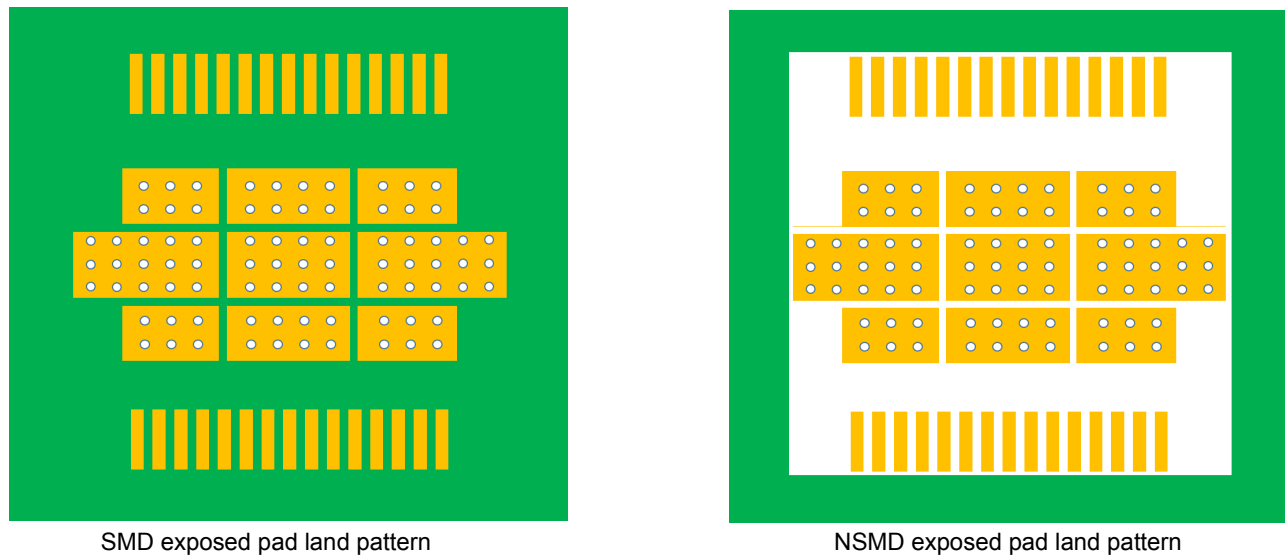


Figure 11. Via placement options for alternative pad options

4.2.5 Pad surface finishes

Almost all PCB finishes are compatible with HSOPs including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn, and Immersion Ag. NXP suggests the PCB surface finish shelf life be monitored to ensure the life has not expired. Surfaces should always be free of contamination and oxidation before PCB assembly.

4.2.6 Solder mask layer

In general, solder mask should be pulled away from both the Input/Output pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area in between the pads show in [Figure 12](#) may be too thin for the solder mask resulting in the solder mask lifting off from the PCB. A potential solution is modification of the solder mask along the pad-to-pad spacing, so only the “toes” of the pads are covered with solder mask for better PCB strength

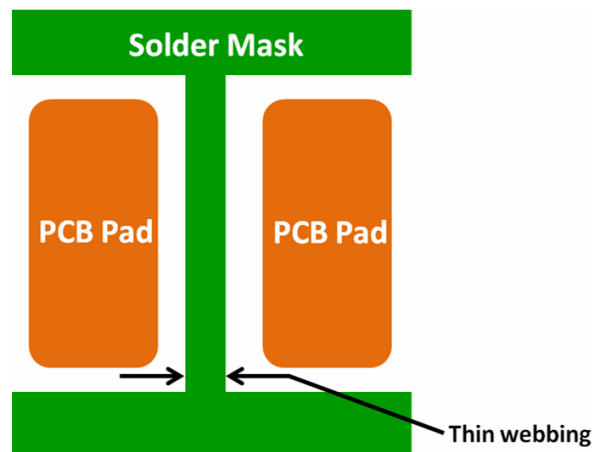


Figure 12. Pad and solder mask with thin webbing

5 Board assembly

5.1 Assembly process flow

A typical surface mount technology (SMT) process flow is shown in [Figure 13](#).

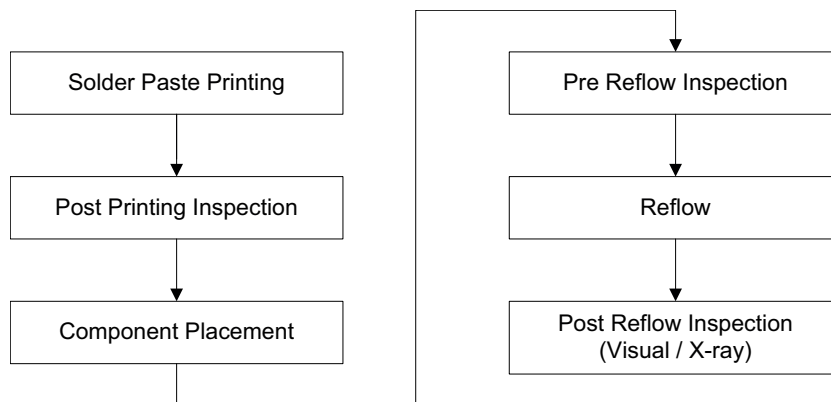


Figure 13. SMT process flow

5.2 Solder stencil/solder paste

For maximum thermal/electrical performance, it is required that the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/electrically enhanced) lead frame based packages, the stencil thickness depends on the lead pitch and package co-planarity. The package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 0.10 mm to 0.15 mm, depending upon the pitch, is recommended. The EP stencil aperture openings should be 0.25 mm smaller than the copper pads on PCB as shown in [Figure 14](#). This allows for proper registration of the stencil to the pad pattern. A large stencil opening may result in poor release. To overcome this, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern. These guidelines results in the solder joint area to be about 80 to 90% of the exposed pad area.

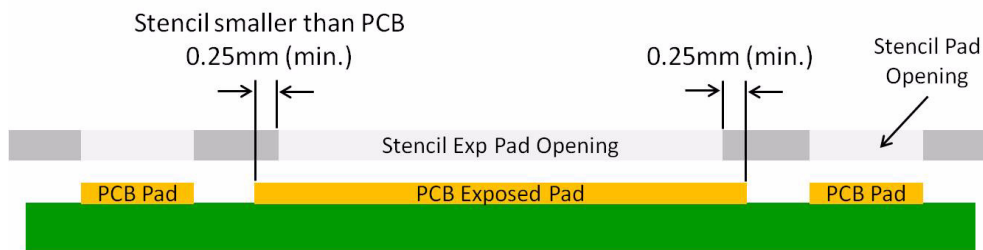


Figure 14. Reduced solder stencil aperture for exposed pad

An array design pattern is recommended in the stencil opening for the large thermal pad region. A large opening or aperture in the thermal region allows “scooping” to occur during screen printing. Other reasons for segmenting the thermal regions include minimizing solder standoff mismatch with terminal pads, minimizing solder voids in the thermal region, and minimizing chances of bridging with terminal pads.

Several different array patterns are being recommended in this section. On HSOP and PQFP packages, stencil thermal openings should be segmented in smaller regions. Examples are shown in [Figure 15](#). The spacing between segments either on the stencil or on the PCB should be 0.15 mm or more. Narrower spacing between segments can become a manufacturing issue.

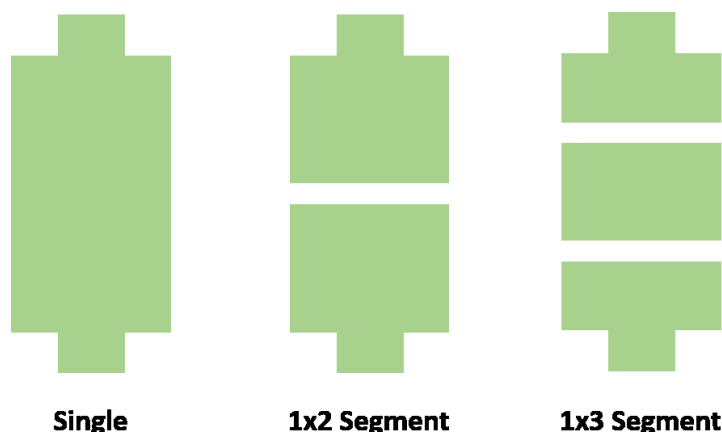


Figure 15. Segmented stencil openings

The stencil opening should be approximately 50% to 80% of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.

5.2.1 Stencil thickness

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board pattern. Due to the fine pitch and small terminal geometry used, care must be taken when printing the solder paste onto the PCB. A 0.125 mm (5.0 mils) thick stainless steel stencil is recommended for 0.50 mm pitch packages. Package pitches greater than 0.65 mm can accommodate a 0.150 mm (6.0 mils) thick stencil.

Solder paste stencil thickness can play a key role in successfully building a PCB. For the large 1.27 mm pitch HSOP, 1.27 mm, thicker stencils are the starting point, 0.125 mm to 0.150 mm (5.0 mils to 6.0 mils). However the thickness decision needs to be balanced by production experiences with the remaining components on the PCB and that may lead to thinner stencils. In cases of thinner stencils, the openings for the large pitch HSOP can be increased. For the small 0.65 mm pitch HSOP and PQFP, the stencil thickness can be between 0.100 mm to 0.125 mm (4.0 to 5.0 mils). There is less of a chance other components on the PCB would suggest an ever thinner stencil.

5.2.2 Solder paste properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering by removing minor surface contamination and oxidation.

There are two different flux systems commonly available.

- The first type requires cleaning, such as standard rosin chemistries and water soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, while the water soluble chemistries are cleaned with pure water.
- The second flux system type requires no cleaning, but normally a little residue remains on the PCB after soldering. The end user should evaluate their entire process and use of no clean flux to ensure desired results.

The spread of solder paste during reflow partially depends upon the solder paste alloy.

5.3 Component placement

The high lead interconnection and insertion density requires precise and accurate placement tools. To meet this requirement, the placement machine should be equipped with optical recognition systems, i.e., vision system, for the centering of the PCB as well as the components during the pick and place motion. A placement accuracy study is recommended to calculate compensations required. NXP follows EIA-481-D standard for tape and reel as well as tube orientation, as shown in [Figure 16](#). See [Section 10.3 Packing of devices, page 21](#), for additional details.

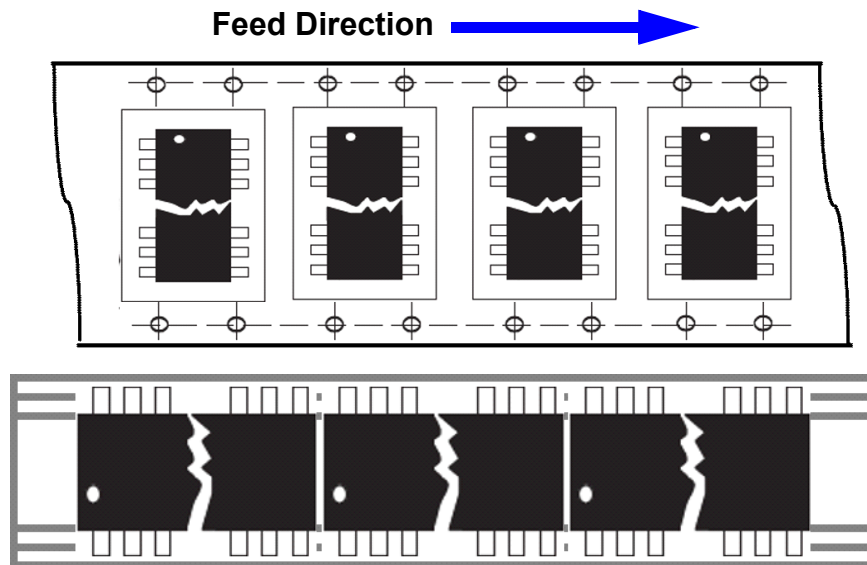


Figure 16. HSOP orientation in tube and tape and reel

5.4 Soldering

Follow the recommendations from the paste manufacturer. Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. In most cases, place thermocouples under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will reach reflow temperatures as well.

Dry air is a common reflow furnace atmosphere. Use nitrogen reflow to improve solderability and to reduce defects (like solder balling). Also, monitor the temperature profile of package top surfaces to validate that the package peak temperature does not exceed the MSL classification for individual devices.

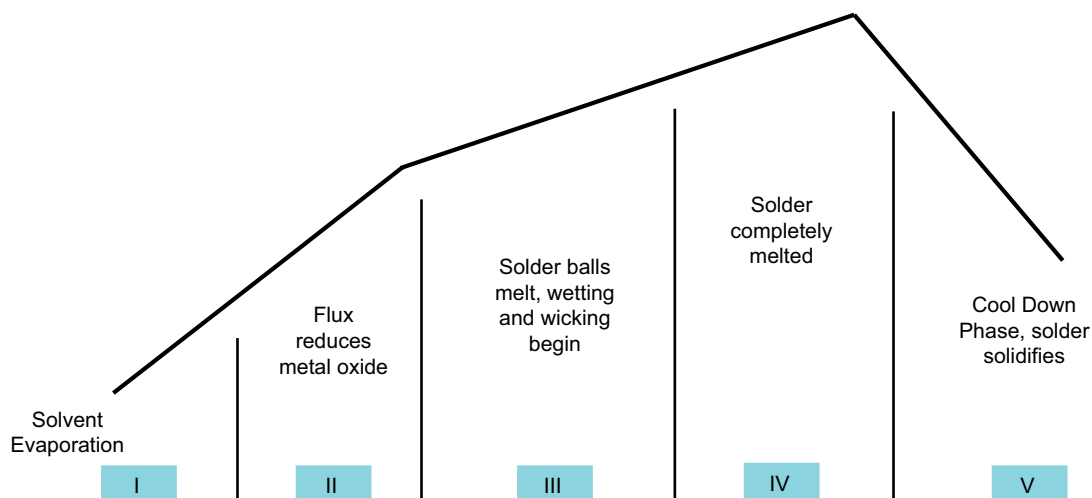


Figure 17. General solder reflow phases

For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a “safety” margin to ensure all solder paste on the PCB reflows.

Deviation from the reflow profile recommended by the paste manufacturer should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as “x” and “y” lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or “x” and “y”. The goal is to have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up. The PCB should be rated for multiple reflows of MSL classification. Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact device used. NXP provides at www.nxp.com, an application note with general comments on reflow profiles. AN3300, General Soldering Temperature Process Guidelines, is a useful starting point.

5.5 Inspection

Whenever possible, using X-ray and other non-destructive vision/optical inspection methods are recommended to verify any open or short-circuit after reflow soldering.

5.6 Common board assembly defects

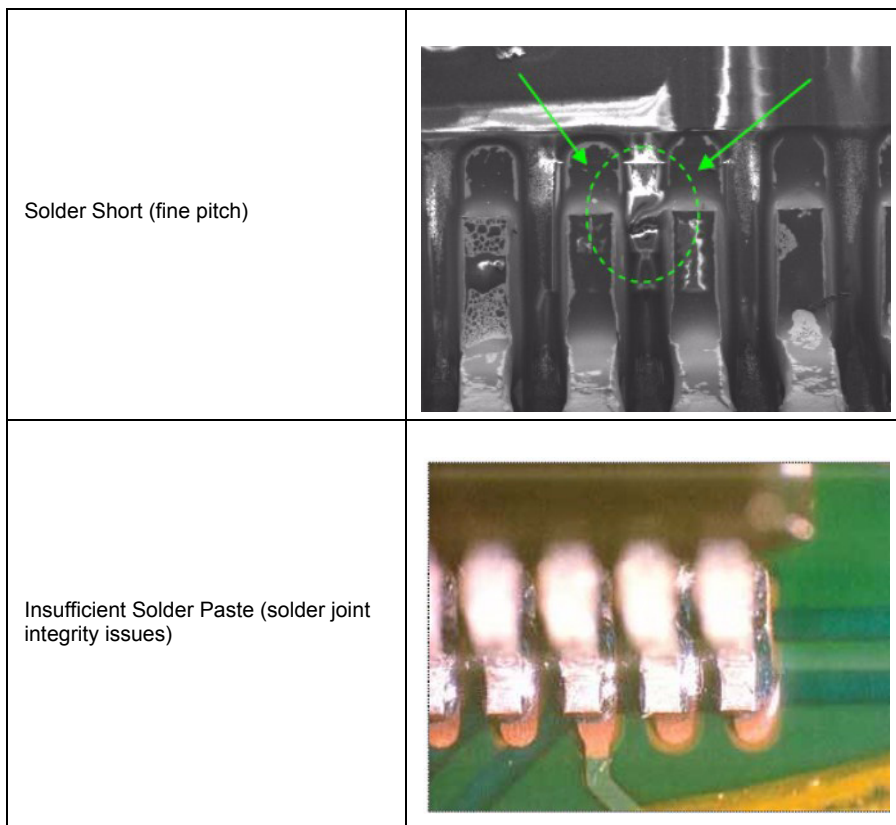


Figure 18. Common board assembly defects

6 Repair and rework procedure

6.1 Repairing

Repair of single solder joints is generally possible, but requires proper tools. A soldering iron can be used to repair soldering defects for packages having leads extending beyond the package periphery, including the HSOP package. Difficulty with fine pitch applications may be observed with the use of soldering irons. The soldering iron temperature and use must be set so the package surface temperature does not exceed its maximum allowable temperature.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced with a new one. This rework can be performed using the heating methods described in the following section.

When performing the rework:

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent package.
- Heating conditions differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- NXP follows industry standard component level qualification requirements which include three solder reflow passes. The three reflow passes simulate board level attach to a double sided board and includes one rework pass. The removed HSOP or PQFP package should be properly disposed of so they do not mix in with new components.

A typical HSOP/PQFP rework flow process is:

1. Tooling preparation
2. Package removal
3. Site redressing
4. Solder paste printing
5. Package remount
6. Reflow soldering

NOTE

Avoid component reuse. NXP's product quality guaranty/warranty does not cover products that have been removed.

In any rework, the PCB is heated. While heating the PCB, take care to observe the thermal limits of the board and its components (e.g. the MSL information.) During heating, the combination of rapid moisture expansion, materials mismatch and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. In order to prevent moisture induced failures, the PCBs and components must be kept in a strictly controlled storage environment (such as dry air or nitrogen). In addition, if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, pre-bake the boards prior to removal of the package. The pre-bake (e.g., 125 °C for 24 hours for boards with SMT components, or 95 °C for 24 hours for boards with temperature sensitive components) removes any moisture that may have accumulated on the board and components during their time out of controlled storage.

Individual process steps for reworking HSOP and PQFP packages are as follows:

6.2.1 Tooling preparation

Various rework systems are available in the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing HSOP and PQFP packages, a system should meet the following requirements:

- **Heating**—Controlled hot air transfer (temperature and air flow) to both the HSOP/PQFP package and its mounted PCB is strongly recommended. The heating must be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side. Nitrogen can be used instead of air. Additional information can be found in [Section 6.2.2 Package removal, page 15](#).
- **Vision system**—The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.

- **Moving and Additional Tools**—Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.2.2 Package removal

If a possibly defective component must be removed from the PCB and returned for analysis, care must be taken during the removal process so as not to introduce further defects that might interfere with failure analysis of the component. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture removal**—Dry bake components before removal at 125 °C for 16 to 24 hours for boards with SMT components or 95 °C for 16 to 24 hours for boards with temperature sensitive components.
- **Temperature Profile**—During de-soldering, ensure the package peak temperature is not higher and temperature ramps are not steeper than the standard assembly reflow process.
- **Mechanics**—Do not to apply high mechanical forces for removal. High force can damage the component and/or the PCB which may limit failure analysis of the package. For large packages, vacuum wands can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

If suspected components are fragile, it is particularly important to determine if they can be electrically tested directly after de-soldering. If the component has to be preconditioned prior to testing (or if safe removal is risky or impossible) the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, apply hot air from the top and bottom heaters. Use an air nozzle of correct size to conduct the heat to the PBGA package so that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater is dependent on the component rating. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress. Therefore, place a bending prevention tool on the bottom of the printed circuit board, and install a bottom heater to allow heating of the entire printed circuit board in order to raise work efficiency.

6.2.3 Site redressing

After the component is removed, the PCB pads have to be cleaned to remove solder residue to prepare for the new component placement. This may be completed by vacuum de-solder, solder sucker, or solder wick braid, etc. after applying flux. Remaining solder residue and projections cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245 °C, which can contribute to PCB pad peeling from the PCB. This is typically a manual operation directly attributed to experience and skill.

Use non-abrasive or soft bristle brushes because abrasive brushes can contribute to bad solder joints (e.g. steel brushes). Prior to placing a new component on the site, apply solder paste (by printing or dispensing) to each PCB pad.

6.2.4 Solder paste printing

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See [Figure 19](#). The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are at close proximity with the HSOP/PQFP components, and the mini-stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled to prevent shorting on the component and/or neighboring components.

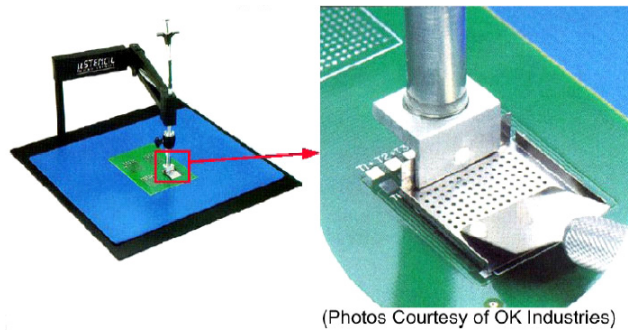


Figure 19. Sample of mini stencil and mini squeegee

6.2.5 Package remount

After preparing the site, the new package can be placed onto the PCB. Handling of the replacement package should also follow the guidelines of [Section 9.2 Moisture sensitivity level, page 20](#). When remounting the package, use rework equipment that has good optical or video vision capability. A split light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY table.

Regular lead array packages exhibit self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. Exposed pads may not exhibit a strong self-alignment capability and precise placement of the component on the PCB is required.

6.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in [Section 5.4 Soldering, page 12](#). Reflow furnaces are not typically used for rework. Rather a dedicated rework station is used which does both part removal and new part joining. During soldering, the package peak temperature and temperature ramps must not exceed those of the standard assembly reflow process.

In IR or convection processes, the temperature can vary greatly across the PCB depending on the furnace type, size and mass of components, and the location of components on the assembly. Additionally, rework stations only apply heat locally, not to the entire PCB. If nozzles are used to direct the heat, the nozzle size must be sufficient large to encompass the entire part. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, carefully attach thermocouples with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

The materials used in rework have a higher potential for creating conductive traces/corrosion etc. compared to standard materials. The PCB might need to be cleaned if it was not cleaned in the “normal” process or if the rework was not done using “no clean” materials.

7 Board level reliability

7.1 Testing details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. Customers may see several different names for board-level reliability (BLR), including second level reliability (2nd level reliability), solder-joint reliability (SJR), and temperature cycling on board (TCoB).

Information provided here is based on experiments executed on HSOP/PQFP devices using a daisy chain configuration. Use actual surface mount process and design optimizations to develop an application specific solution.

- For automotive grade product applications, the widely accepted temperature range for testing is -40 °C to +125 °C.
- Consumer SJR temperature cycling conditions may vary widely depending on the application and specific user. Typically, NXP consumer SJR testing is performed from 0 °C to +100 °C.

The preferred test method varies by market and industry. For automotive, the primary test is a version of IPC-9701A, air temperature cycling. For the consumer market, JEDEC's drop test is the primary test (JESD22-B111). Telecommunications uses both IPC-9701A and IPC-9702 (monotonic bend). NXP may not test each specific electronic package configuration and may not have all the tests for each market and industry.

Table 4 shows the NXP standard test set-up for performing board level solder joint reliability testing.

Table 4. Board level reliability setup

Board level reliability testing: material and test setup	
PCB Board	1.58 mm thickness 4.0 Cu layer OSP surface finish
Test Board Assembly	Pb-free solder paste SAC387 Reflow peak temperature for SAC assembly ~ 240 °C Pb solder paste Sn63Pb37 Reflow peak temperature for SnPb assembly ~ 220 °C 0.100 mm thickness, Ni plated, laser cut and electro-polished stainless steel stencil
Cycling conditions	Continuous in-situ daisy chain monitoring per IPC-9701A and IPC-SM-785 Air Temperature Cycling (ATC) for Automotive <ul style="list-style-type: none"> • -40 °C/+125 °C • 15 minute ramp/15 minute dwell • 1.0 hour cycle time Air Temperature Cycling (ATC) for Commercial & Industrial <ul style="list-style-type: none"> • 0 °C/+100 °C • 10 minute ramp/10 minute dwell • 1.0 hour cycle time
Package Test Vehicle	Production BOM package including die (die mechanically present, without wire bond connection) Daisy chain bond pattern on the lead frame to allow continuous monitoring

7.2 Solder joint reliability results

NXP experimentally gathers board-level reliability data for a variety of packages. To get results from these experiments (including Weibull plots) contact the NXP sales team. Customers should interpret the NXP solder joint reliability data to see how well they meet the final application requirements.

8 Thermal characteristics

8.1 General thermal performance

Since the thermal performance of the package in the final application depends on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by NXP should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, NXP recommends running application specific thermal calculations in the design phase to confirm the on-board thermal performance.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific, and depends on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

8.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Additional factors that need be considered in PCB design and thermal rating of the final application amongst others are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints which may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

NXP product data sheets document the appropriate thermal properties of individual products. Product data sheets are available at www.nxp.com. More detailed thermal properties may be requested by customers.

8.3 Package thermal properties - definition

The thermal performance of HSOP and PQFP packages are typically specified by definition of thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$, and Ψ_{JT} (in °C/W). Thermal characterization is obtained using physical measurement and by running complex simulation models under the following conditions:

- Two thermal board types:
 - Single layer board (1s) per JEDEC JESD51-3 & JESD51-5 (exposed pad packages only)
 - Four layer board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only).
- Four boundary conditions:
 - Natural convection (still air) per JEDEC JESD51-2
 - Forced convection per JEDEC JESD51-6
 - Thermal test board on ring style cold plate method per JEDEC JESD51-8
 - Cold plate method per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value measuring the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into and through the test board followed by convection and radiation off the exposed board surfaces.

8.3.2 $R_{\theta JMA}$: theta junction-to-moving-air forced convection

Junction-to-Moving-Air (Theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JMA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to moving air (at 200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: theta junction-to-board

Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a high effective thermal conductivity four layer test board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only) on a ring style cold plate. $R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta JC}$: theta junction-to-case

Junction-to-Case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface, as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case is defined as either the temperature at the top of the package (for non-exposed pad packages), or the temperature at the bottom of the exposed pad surface (for exposed pad packages). For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 Ψ_{JT} (Psi JT): junction-to-package top

Junction-to-Package top (Psi JT or Ψ_{JT}) indicates the temperature difference between package top and the junction temperature, optionally measured in still air condition (per JEDEC JESD51-2) or forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be mixed up with the parameter $R_{\theta JC}$: $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while Ψ_{JT} is the value of the temperature difference between package surface and junction temperature, usually in natural convection.

8.4 Package thermal properties - example

An example of the thermal characteristics as typically shown in the NXP product data sheet, is shown in Table 5. The example applies to a package size HSOP 20LD, Pitch 1.27mm, Die size ~ 5.54 mm x 4.19 mm.

Table 5. Thermal resistance example

Rating	Board type	Thermal resistance	Value	Unit	Notes
Junction to Ambient (Natural Convection)	Single Layer board (1s)	$R_{\theta JA}$	52	°C/W	(1), (2)
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JA}$	19	°C/W	(1), (2)
Junction to Board	---	$R_{\theta JB}$	3.0	°C/W	(3)
Junction to Case (Bottom)	---	$R_{\theta JC}$ (Bottom)	0.2	°C/W	(4)
Junction to Package (Top)	Natural Convection	Ψ_{JT}	5.0	°C/W	(5)

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
- Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9 Case outline drawing, MCDS and MSL rating

9.1 Case outline drawing, MCDS and MSL information download

NXP offers packaging, environmental and compliance information at www.nxp.com, both in the parametric tables and in the device information details. Select the package type hyperlink of the specific part number of interest or enter the part number in the search box and review the part details. The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752 reporting format, can be downloaded as a PDF file. Information on product specific moisture sensitivity level (MSL) is also available in the part details.

9.2 Moisture sensitivity level

The moisture sensitivity level (MSL) indicates the floor life of the component and its storage conditions and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or lead-frame, wire bond damage, die damage, and internal cracks. In the most severe cases, the component bulges and pops, known as the “popcorn” effect.

Moisture-sensitive components must be dried and sealed in a moisture barrier antistatic bag with a desiccant and a moisture indicator card. The antistatic bag must be vacuum sealed according to IPC/JEDEC J-STD-033 and the component must not be removed until immediately prior to assembly to the PCB.

Table 6 presents the MSL definitions per IPC/JEDEC's J-STD-20. Refer to the “Moisture Sensitivity Caution Label” on the packing material, containing information about the moisture sensitivity level of NXP products. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and the maximum reflow temperature which must not be exceeded during board assembly at the customer's facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components are required to be baked prior to the assembly process. Refer to imprints/labels on the respective packing to determine allowable maximum temperature.

The higher the MSL value, the more attention is needed to store the components. NXP packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package. Table 7 depicts the best case MSL for each package size at the time of this document's release. NXP packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

Table 6. MSL descriptions

Level Rating	Floor life	
	Time	Conditions
1	Unlimited	30 °C / 85% RH
2	1 Year	30 °C / 60% RH
2a	4 Weeks	30 °C / 60% RH
3	168 Hours	30 °C / 60% RH
4	72 Hours	30 °C / 60% RH
5	48 Hours	30 °C / 60% RH
5a	24 Hours	30 °C / 60% RH
6	Time on Label (TOL)	30 °C / 60% RH

Table 7. MSL capability of HSOP and PQFP packages

Package type	Package body size (W)	Package body size (L)	MSL level	PPT
HSOP 20	11.0	15.90	3	245 °C
HSOP 30	11.0	15.90	3	245 °C
HSOP 44	11.0	15.90	3	245 °C
PQFP 64	14.0	14.0	3	245 °C

10 Package handling

10.1 Handling electrostatic discharge sensitive devices

Semiconductor integrated circuits (ICs) and components are electrostatic discharge sensitive devices (ESDS) and proper precautions are required for handling and processing them. Electrostatic discharge (ESD) is one of significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing must be considered.

The following industry standards describe detailed requirements for proper ESD controls. NXP recommends users to meet the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD625-A - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-61340-5 - Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling moisture sensitive surface mount devices

HSOP and PQFP packages are moisture/reflow sensitive surface mount devices (SMD) and proper precautions are required for handling, packing, shipping, and use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures higher than 200 °C. As noted in [Section 9.2 Moisture sensitivity level, page 20](#), during solder reflow, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability concern, and proper handling of SMDs must be considered.

Dried moisture sensitive SMDs are placed in tray or tape-and-reel, and dry packed for proper transportation and storage. SMDs are sealed with desiccant material and a humidity indicator card inside of a moisture-barrier bag (MBB). The shelf life of dry packed SMDs is 12 months from the dry pack seal date when stored in < 40 °C/90%RH environment.

Proper use and storage of moisture sensitive SMDs are required after the MBB is opened. Improper use and storage increases various quality and reliability risks. SMDs subjected to reflow solder or other high temperature process must be mounted within the period of floor environment specified by MSL, or stored per J-STD-033 standard.

Baking SMDs is required before mounting if any of followings are experienced.

- SMDs exposed to specified floor environment greater than the specified period
- Humidity indicator card reading > 10% for level 2a - 5a or > 60% for level 2 devices when read at 23 °C ± -5.0 °C environment.
- SMDs are not stored according to J-STD-033 standard

Baking procedure, and more detailed requirements and procedures of handling Moisture Sensitive SMDs can be found in the following industry standard.

- PC/JEDEC J-STD-033 - Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Device.

10.3 Packing of devices

HSOP devices are contained in Tube or Tape-and-Reel, and PQFP devices are contained in a Tray configuration. Tube, Tape-and-Reel, and Tray are dry packed for transportation and storage. Packing media are design to protect devices from electrical, mechanical, and chemical damages as well as moisture absorption, but proper handling and storage of dry packs is recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90%RH environment, excessive stacking of dry packs, etc.) increases various quality and reliability risks.

- TUBES (also commonly referred to as Magazines or Rails)
 - Materials: Shipping tubes shall be manufactured of PVC (Poly Vinyl Chloride) or PS (Polystyrene) or PC (Poly Carbonate) materials dipped with an anti-static solution provides anti-static capability.
 - NXP's tube designs fit standard Jedec package designs - See [Table 8](#)
 - Pin one orientation end: The preferred pin one plug (tube/ magazine insertion end) must be green. IMPORTANT NOTE: If pin one indication is NOT required; then both ends must be of the same color from one of the following allowed colors: clear, grey, white, or black.
 - Opposite pin one (also referred to as hold or tack or anchor): The preferred color must be clear, grey, white, or black.
 - Examples of single and multiple tube packing configurations shown in [Figure 20](#) and [Figure 21](#) respectively.

Table 8. JEDEC tube example

Package	Tube section	Tube width/length	Plug
HSOP 20			
HSOP 30			
HSOP 44			

Packaging Method For Single Tube In Dry Pack Using Insert

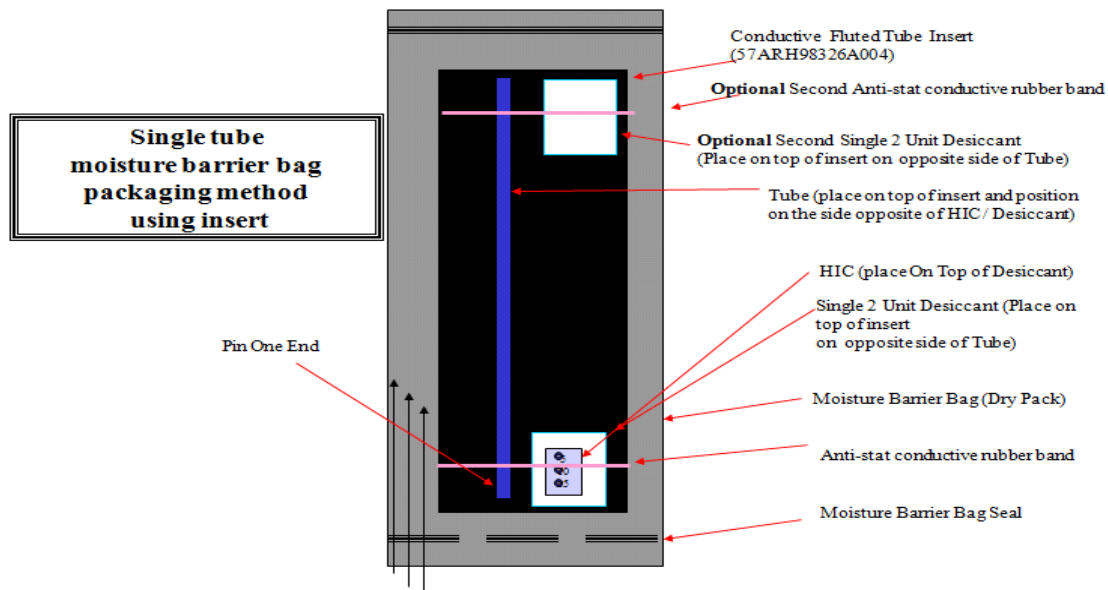


Figure 20. Sample of single tube packing method

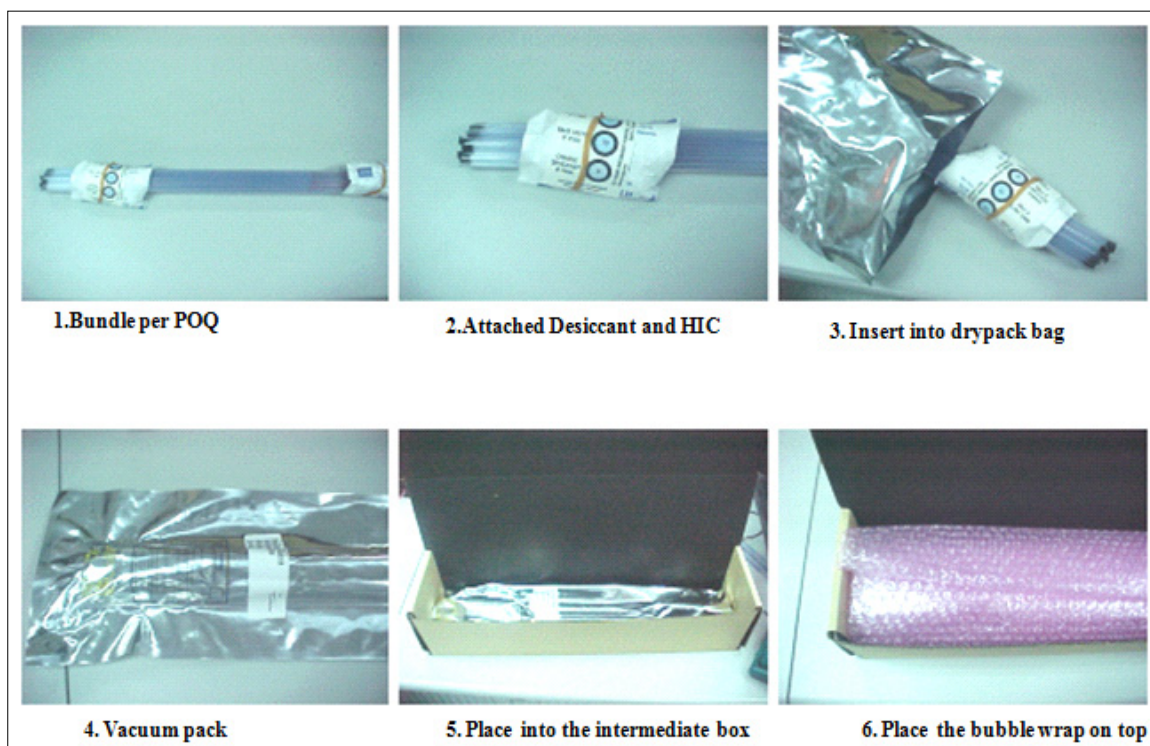


Figure 21. Sample of multiple tube packing method

- Tray
 - NXP complies with standard JEDEC tray design configuration - See [Figure 22](#)
 - Pin one of devices is oriented with lead one toward the chamfered corner of the tray
 - Trays designed to be baked for moisture sensitive SMDs, but temperature rating of tray must NOT be exceeded when devices are baked. Temperature rating can be found at end-tab of tray. Recommended baking temperature of trays is 125 °C.
 - Trays are typically banded together with 5+1 (five fully loaded trays and one cover tray) stacking and dry packed in moisture barrier bag. Partial stacking (1+1, 2+1, etc.) is also available, depending on individual requirements.

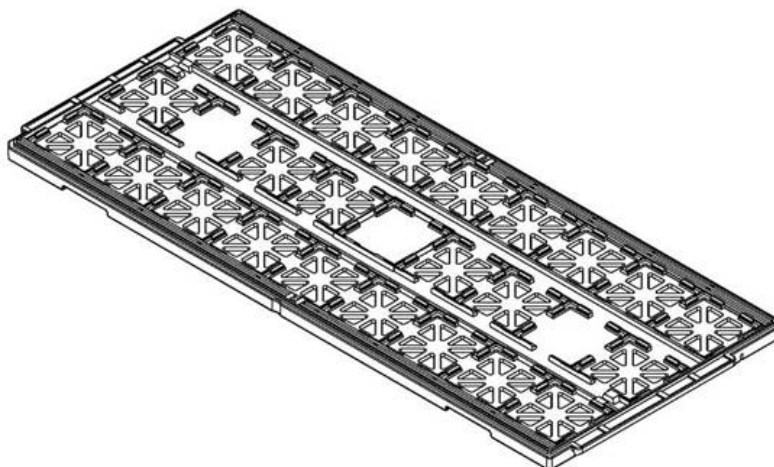


Figure 22. JEDEC tray example

- Tape and reel
 - NXP complies with EIA-481D for carrier tape and reel configuration and orientation - See [Figure 23](#)
 - Tape and Reels are NOT designed to be baked at high temperature
 - Each Tape and Reel is typically dry packed in moisture barrier bag

11 References

[1]	IPC/JEDEC J-STD-020, Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, July 2004.
[2]	IPC/JEDEC J-STD-033, Joint IPC/JEDEC Standard for handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices, February 2012
[3]	EIA-783, Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation), November 1998.
[4]	EIA/JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), December 1995.
[5]	EIA/JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board, October 1999.
[6]	EIA/JESD 51-6, Integrated Circuits Thermal Test Method Environment Conditions - Forced Convection (Moving Air), March 1999.
[7]	MIL SPEC-883 Method 1012.1, Thermal characteristics, February 2006.
[8]	IPC-7351B, Generic Requirements for Surface Mount Design and Land Pattern Standards, June 2010.
[9]	IPC-9701A, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, February 2006.
[10]	IPC/JEDEC-9702, Monotonic Bend Characterization of Board-Level Interconnects, June 2004
[11]	IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, November 1992.
[12]	JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, July 2003.
[13]	IPC-1752, Materials Declaration Management, June 2005.
[14]	EIA-481, Standards - Excerpts used to assure complete alignment.
[15]	JESD615-A, Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.
[16]	IEC-101/61340-5, Specification for the Protection of Electronic Devices from Electrostatic Phenomena.
[17]	MO-166, Plastic Small Outline Heatslug Package, JEDEC Solid State Product Outline.

12 Revision history

Revision	Date	Description of Changes
1.0	12/2005	<ul style="list-style-type: none">Initial release
2.0	10/2015	<ul style="list-style-type: none">Multiple revisions
3.0	12/2015	<ul style="list-style-type: none">Updated Figure 5Added Table 3
	7/2016	<ul style="list-style-type: none">Updated NXP document form and style

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