AN11401

TEA1720/TEA1705 5 W to 12.5 W power supply/USB charger

Rev. 1 — 5 December 2013 Application note

Document information

Info	Content
Keywords	ultra low standby power, constant output voltage, constant output current, primary sensing, Integrated emitter switch, low-cost NPN high-voltage switch, integrated high voltage start-up, USB charger, standby supply, 5 W to 12.5 W supply, transient controller companion
Abstract	The TEA1720 is a primary sensing controller for power supplies up to 12.5 W. A low-cost NPN transistor is used as high-voltage switch. The no-load power can be as low as 20 mW for a 10 W charger. It surpasses the Energy Star 5 level (30 mW). Excellent transient response can be achieved when using the transient controller TEA1705 on secondary side. When the maximum output power is exceeded, the IC changes from constant voltage mode to constant current mode, which is suitable for battery charging.

Revision history

Rev	Date	Description
v.1	20131205	first issue

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

The TEA1720 is a flyback controller with primary sensing and an integrated emitter switch for driving a low-cost NPN high-voltage switch.

An advanced burst mode and integrated high-voltage start-up circuit ensure a very low no-load power consumption of 20 mW for a 10 W mobile charger.

Excellent transient response in burst mode can be achieved by using the (optional) TEA1705 transient controller on secondary side. Using a wake-up pulse that travels through the flyback transformer, the TEA1705 IC triggers the TEA1720 on the primary side to recommence switching when the output voltage (V_{out}) drops to below 4.9 V.

When the maximum output power level is reached, the constant output voltage control mechanism changes to a constant output current control mechanism, enabling the TEA1720 to be used as a constant current charger.

Depending on the dimensioning of the mobile charger circuit, the output power range can typically be 5 W to 12.5 W. Choose the NPN BJT switch accordingly.

The TEA1720 is assembled in an SO8 package. The (optional) TEA1705 comes in a SOT23 package.

All values mentioned in the application note are typical values. For the minimum/maximum values and spread figures, see the *TEA1720 and TEA1705 data sheets*.

2. Scope

This application note describes application aspects of the TEA1720 SMPS controller IC. The IC is typically used for low-power adapter or USB mobile charger applications. The functionality, the control functions and the basic dimensioning of the circuit components of an application circuit using the TEA1720 controller and optionally a TEA1705 transient controller are explained.

Detailed transformer calculation is available in a separate calculation sheet.

3. TEA1720/TEA1705 low-power adapter

The features of the TEA1720 enable power engineers to design a reliable, cost-effective, and efficient adapter supplies with low no-load power consumption and a low component count. The optional TEA1705 realizes excellent transient response in burst mode without requiring an optocoupler or other additional mains isolation crossing components.

3.1 Key features TEA1720

3.1.1 Power features

- Low component count for cost-effective design
- Highly efficient > 80 %
- Primary sensing for control of the output voltage without optocoupler and secondary feedback circuitry
- Built-in emitter switch for driving a low-cost NPN high-voltage bipolar transistor
- Minimizes audible noise in all operation modes
- Energy Star 2.0 compliant
- USB 1.1 and 1.2 compliant for mobile phone chargers
- Jitter function for reduced EMI
- Versions available with built-in cable compensation
- Available in SO8 package

3.1.2 Green features

- No-load power consumption < 20 mW
- Very low supply current in no-load condition with energy save mode
- Incorporates a high-voltage start-up circuit with zero current consumption at normal switching operation

3.1.3 Protection features

- OverVoltage Protection (OVP) with auto-restart
- UnderVoltage LockOut (UVLO) on the IC supply pin
- OverTemperature Protection (OTP)
- SENSE pin short circuit protection
- Hiccup feature for automatic switch-off at output voltage that is continuously too low
- Demagnetization protection for guaranteed Discontinuous Conduction Mode (DCM) operation
- Open and short-circuit protection of the feedback control pin (FB)
- Short circuit protection of the charger output

3.2 Key features TEA1705

3.2.1 Power features

- Excellent transient response in burst mode by constant monitoring of the output voltage (V_{out}) and waking up the TEA1720 on primary side via the transformer when V_{out} drops to below 4.9 V.
- Only two external components required
- No additional mains isolation crossing components required
- Available in SOT23 package

3.2.2 Protection features

- Preventing V_o to exceed 6.3 V in a no-load condition by drawing additional current (up to 15 mA at 6.3 V) to protect the output capacitors when V_o exceeds 5.9 V when the preload resistor provides insufficient load.

3.3 Applications

- Mobile communication
  - Mobile phone battery charger
  - Smart phone battery charger
  - Tablet computer battery charger
- Major home appliances
  - Washing machines and dryers
  - Refrigerators and freezers
  - Dish washers
  - Induction cookers
  - Room air conditioners
- Computing and consumer
  - E-readers
  - Portable audio/video
  - Settop boxes
  - PC peripherals
  - Standby power supply for PC and TV
- Industrial and residential
  - Smart metering
  - Lighting
  - Home and building automation
  - Heating, Ventilation, and Air Conditioning (HVAC)
  - Industrial automation and control

4. Basic application schematic

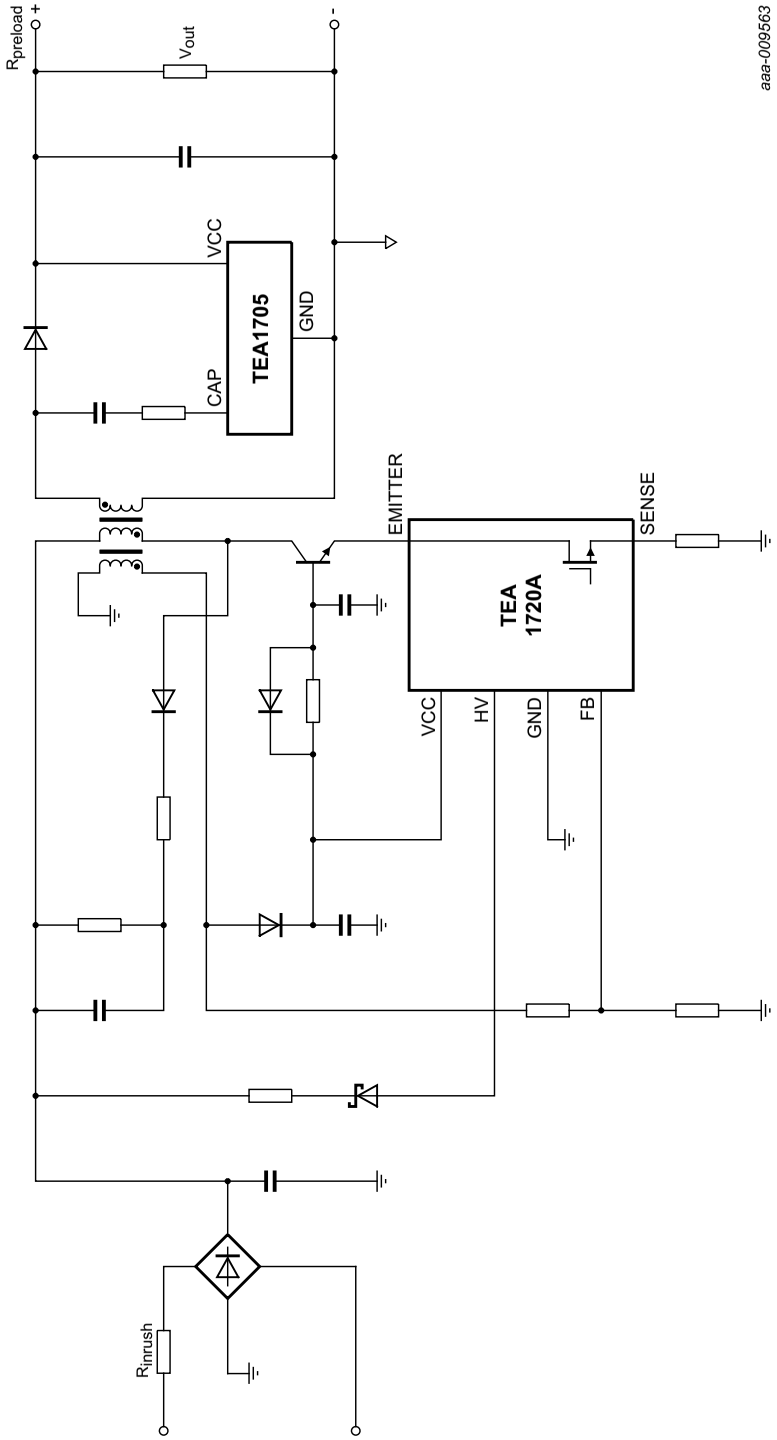


Fig 1. Basic application schematic

5. Pinning

5.1 TEA1720

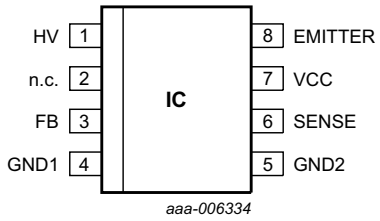


Fig 2. TEA1720 pinning diagram (S08)

Table 1. Pin description

Pin	Pin name	Description
1	HV	input high voltage startup current source; breakdown voltage is 500 V
2	n.c.	not connected; high-voltage spacer pin
3	FB	feedback input; senses the voltage on the aux winding during secondary stroke (which represents the voltage on the output winding) via a resistive divider at constant output voltage the sensed voltage is regulated on 2.5 V when the sensed voltage drops to below 2.5 V, the regulation changes to constant current mode under 1.1 V, the controller enters hiccup mode (short circuit protection) the OVP protection level is 3.2 V demagnetization detection (which releases the next stroke and guarantees discontinuous operation) checks that the voltage on the auxiliary winding drops to below 50 mV after the secondary stroke
4; 5	GND	ground connection
6	SENSE	connected to the source of the internal MOSFET which is used as emitter switch; the current through the MOSFET and the serially connected NPN transistor is monitored using a resistor from the SENSE pin to ground the peak level in burst mode is approximately 120 mV; the peak level in other modes ranges from 120 mV and 530 mV (exact values are depending on the dV/dt on the source pin)
7	VCC	supply voltage at start-up, an internal current source charges the connected VCC capacitor until the V_{start} level (17 V) is reached the device starts switching and the auxiliary winding takes over the supply The UnderVoltage LockOut level (UVLO) on the VCC pin is 8.5 V
8	EMITTER	drain connection of the internal MOSFET used as emitter switch; the breakdown voltage is 40 V. R_{DSon} is 0.9 Ω

5.2 TEA1705

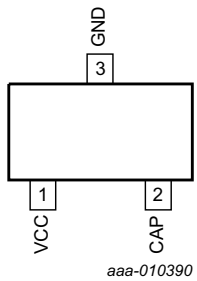


Fig 3. TEA1705 pinning diagram (S0T23)

Table 2. Pin description

Pin	Pin name	Description
1	VCC	supply voltage and level monitoring of V_{out} when V_{CC} drops to below 4.9 V and no switching occurs, a pulse is generated to wake-up the TEA1720 on primary side to protect polymer electrolytic capacitors with 6.3 V rating when no preload resistor is connected or the preload resistor provides insufficient load, the supply current increases linearly to 15 mA at 6.3 V when V_{CC} exceeds 5.9 V
2	CAP	connection communication capacitor the communication capacitor is discharged when V_{CC} drops to below 4.9 V while no switching occurs during switching, the communication capacitor is (re)charged via this pin
3	GND	ground connection

6. System description

This section describes the system. Use Figure 1 as reference throughout this section.

6.1 Supply

At start-up, an internal current source, connected to the HV pin, charges the capacitor connected to the VCC pin (see Figure 4).

When the voltage level on the VCC pin reaches 17 V ($V_{CC(startup)}$), the internal current source is switched off. The IC starts switching. The internal MOSFET drives the external NPN via emitter switching. Both the IC supply current and the base current for the NPN are delivered by the charge stored in the capacitor connected to the VCC pin.

When switching starts, the voltage generated at the auxiliary supply winding of the transformer provides the supply (see Figure 5 and Figure 6).

When the IC does not start switching (due to protection) or when the auxiliary winding does not take over the supply voltage, the voltage on the capacitor on the VCC pin drops to 8.5 V ($V_{CC(stop)}$). The internal current source is enabled again. It charges the capacitor to 17 V ($V_{CC(start)}$). This sequence is repeated (see Figure 6).

It is also possible to supply the IC externally. But the supply voltage must exceed 17 V ($V_{CC(startup)}$) with some margin to guarantee a start-up.

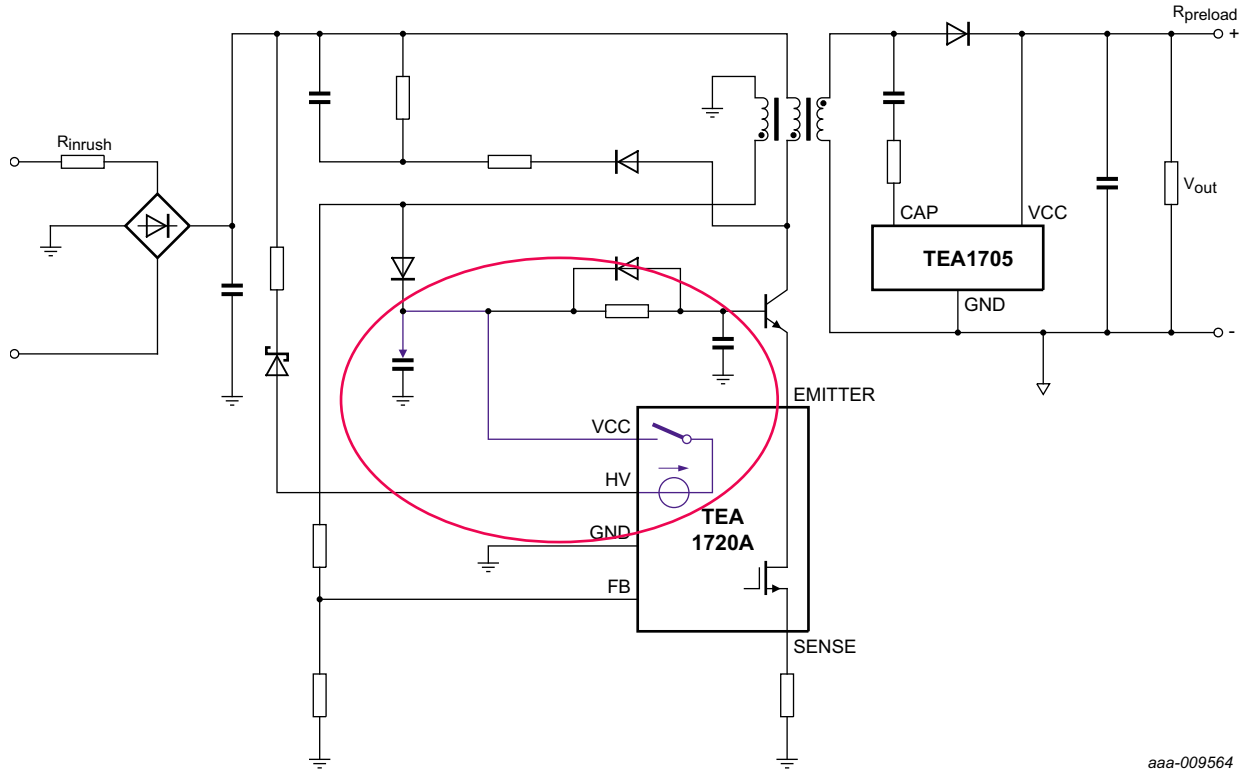


Fig 4. Charging the VCC capacitor

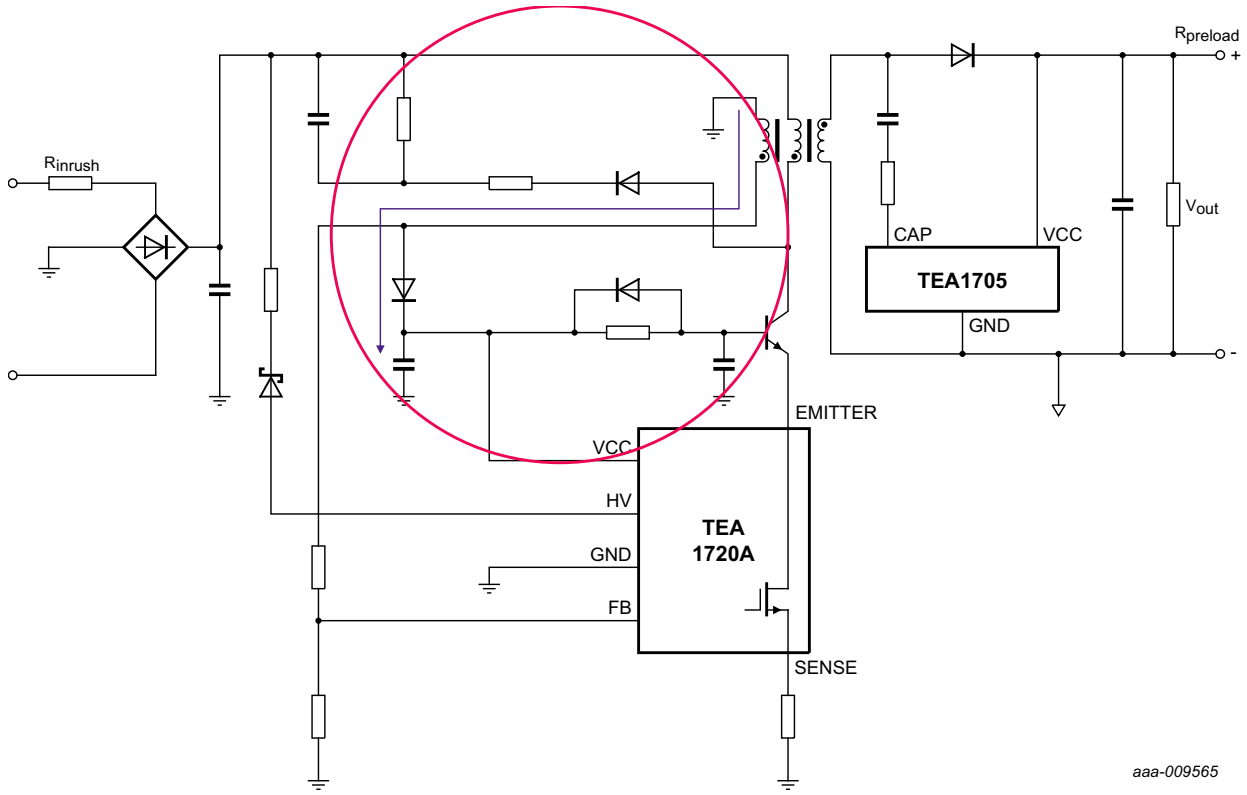
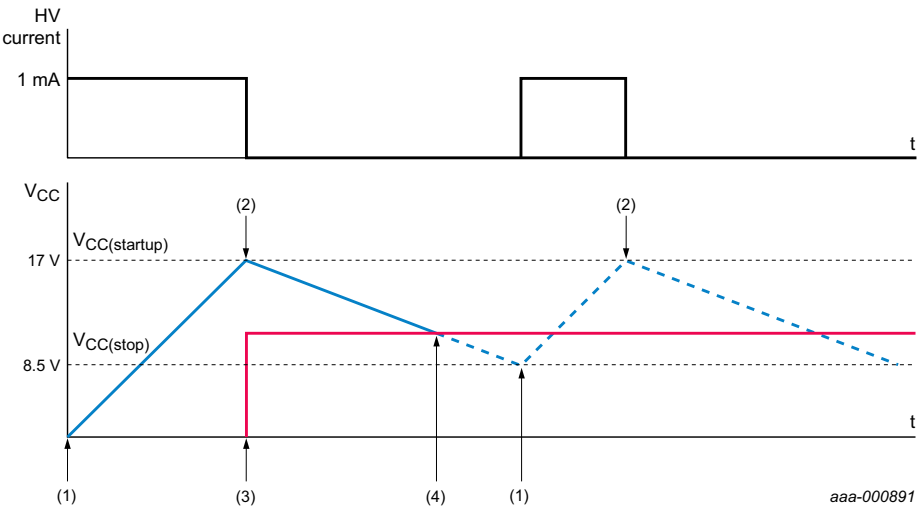


Fig 5. Rectified voltage of auxiliary winding takes over the VCC supply



(1) HV current source on

(2) HV current source off

(3) Switching start; V_{aux} builds up

(4) V_{aux} takes over VCC supply

Fig 6. Voltage on the VCC pin

6.2 Operating modes

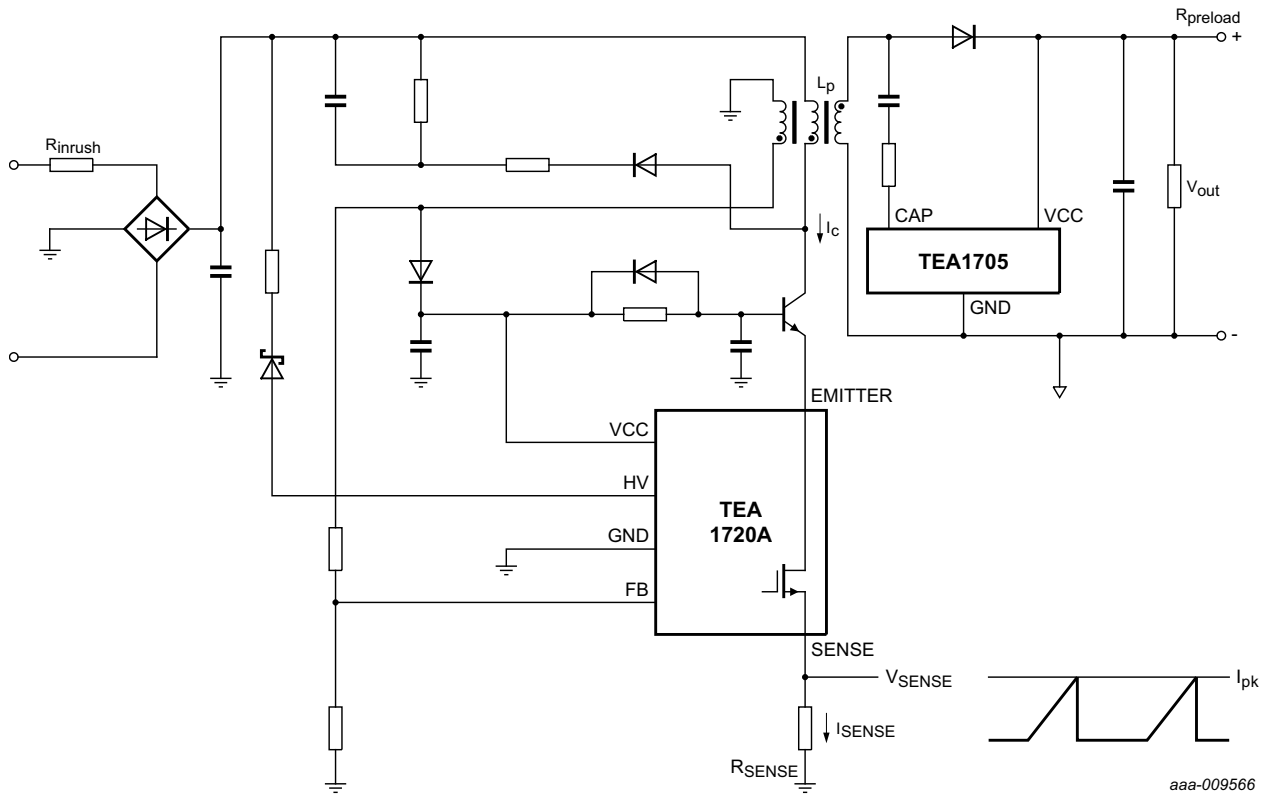


Fig 7. Basic circuit with relevant parameters

From no-load to maximum load and in Constant Current (CC) mode, the TEA172x uses different operating modes, which are explained below.

A simplified model is used to explain the different modes (see Figure 14). The assumption is that the current I_{SENSE} in the sense resistor R_{SENSE} equals the collector current (I_c) of the NPN. In reality, I_{SENSE} deviates from I_c because of the additional base current flowing through resistor R_{SENSE}. Moreover, the peak value of I_c exceeds I_{SENSE} due to delayed switch-off of the NPN transistor (caused by storage time).

For all these items compensations are built in the TEA1720. Details of the emitter drive are explained in Section 6.3.

The regulation of a flyback converter is based on regulating the transferred energy according to Equation 1:

$$P_{out} = 0.5 \times L_p \times I_{pk}^{2} \times f_{sw} \times \eta \quad (1)$$

Where:

- P_{out} = output power
- L_p = transformer primary inductance
- I_{pk} = peak value of the primary current at NPN switch-off time

- f_{sw} = switching frequency
- η = converter efficiency

The output power equals the energy, stored per stroke in the transformer ($0.5 \times L_p \times I_{pk}^2$) times the number of strokes per second (f_{sw}) minus the losses (efficiency η).

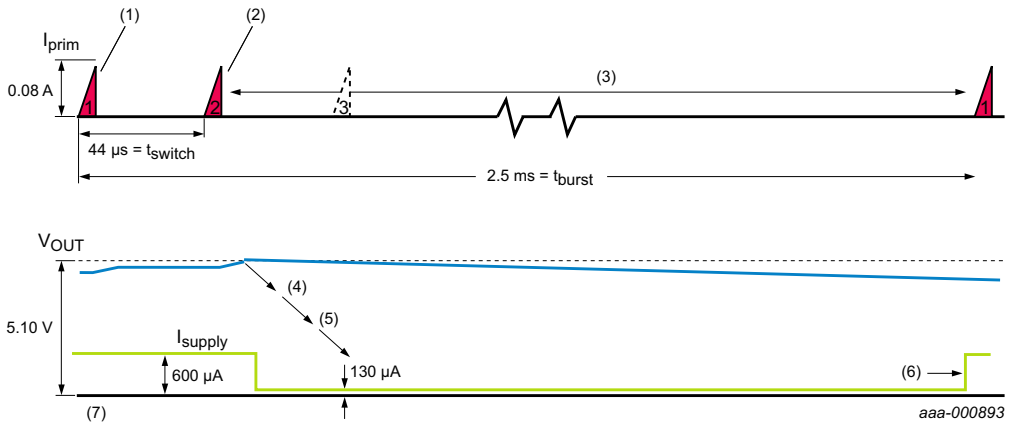
Though not completely accurate, this basic formula is sufficient to understand the control modes.

The different operating modes are:

- Burst mode
- CVC mode: Constant Voltage peak Current regulation control
- CVF mode: Constant Voltage Frequency regulation control
- CCF mode: Constant Current Frequency regulation control

6.2.1 Burst mode

At fixed time intervals, the burst period is started. Each burst period starts with one stroke at a fixed I_{pk} level. After the stroke the voltage is sensed at the FB pin near the end of the secondary stroke. If the sensed voltage equals or exceeds 2.5 V, no additional strokes are made. The IC enters energy save mode until the next burst period. If the sensed voltage at the FB pin is < 2.5 V, additional strokes are made until the sensed voltage level at the FB pin exceeds 2.5 V. Then the IC enters energy save mode until the next burst period.



(1) Start of burst
(2) End of burst
(3) Minimum supply current for energy save; Only the oscillator is active
(4) Vout(pk) reaches control value in 1 or 2 cycles
(5) IC switches to minimum supply current, energy save
(6) IC switches to nominal supply just before new burst start

Timing and currents given are for TEA1720 version with f_{burst} = 400 Hz

Fig 8. Burst mode with energy save mode

The low no-load power is achieved by:

- Low burst period repetition rate (400 Hz)
- The IC enters energy save mode between burst periods, reducing current consumption by a factor of 4.5

Audible noise is limited by:

- Selecting the minimal I_{pk} ($I_{pk(min)}$) for burst mode
- Repetition rate of strokes within the burst period is 22.5 kHz; well above the audible limit

The no-load power is < 20 mW for a 10 W charger. At lower output power, lower no-load power can be achieved.

The fixed time interval between burst periods determines the no-load power but also the size of the required output capacitors. For more information about the size of the output capacitor related to output power, ripple and load step performance (see Section 6.5).

When the output load increases, more strokes per burst period are added to transfer enough energy.

Finally, the whole burst period is filled with strokes and the IC is switching continuously. When the load increases further, the IC enters the CVC (Constant Voltage peak Current control) mode.

To reduce the ripple in burst mode, slope compensation is added when the number of strokes exceeds 50 % of the burst period.

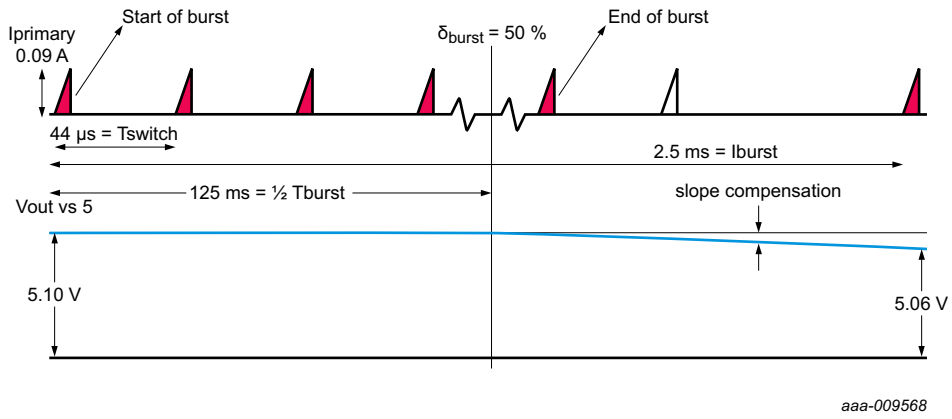


Fig 9. Slope compensation

For duty cycles > 50 %, the reference level of V_{out} is linearly decreased. This ensures that the regulation converges and the duty cycle remains constant. Figure 10 shows a graphical explanation.

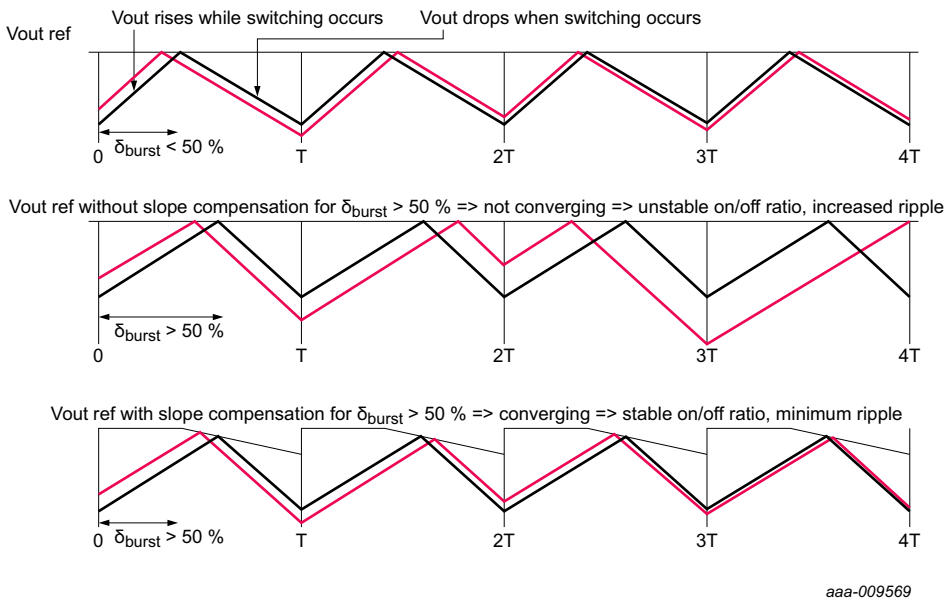


Fig 10. Slope compensation regulation

In all graphs the black line represents the output voltage when the regulation is stable. The red line represents the output voltage when there is a disturbance and the loop has to regulate back to the stable state.

In burst mode, strokes are made and V_{out} increases until the reference level of V_{out} is reached. Switching stops and the load discharges the output capacitor until the next burst period starts.

When δ < 50 % (Figure 10 top graph), the regulation converges to the stable state after a disturbance.

When δ > 50 % and no slope compensation is present (Figure 10 middle graph), the loop does not converge and the δ varies between minimum and maximum (1 stroke/burst and 31 strokes/burst). The long idle time after a burst period with 1 stroke causes increased ripple at higher loads due to the longer discharge time of the output capacitor.

When δ > 50 % and slope compensation is present (Figure 10 bottom graph), the reference level for V_{out} drops linearly for 50 % < δ < 100 %.The regulation converges and the ripple of V_{out} remains minimal.

P_{out} in burst mode can be calculated with Equation 2:

$$P_{out} = 0.5 \times L_p \times I_{pk(min)} \times f_{burst} \times average\_no\_of\_strokes\_per\_burst \times \eta \quad (2)$$

Where:

- f_{burst} = fixed burst frequency, which determines the fixed time interval between bursts
- $I_{pk(min)}$ = fixed minimum I_{pk} level in burst mode

Measuring the voltage over the resistor from the SENSE pin to ground determines the level of I_{pk}. The peak level voltage is around 120 mV in the application.

6.2.2 CVC mode

The CVC mode (Constant Voltage peak Current regulation mode) starts where the burst mode ends. The IC is continuously switching at the repetition rate of strokes within the burst period (= 22.5 kHz = f_{min}, the minimum switching frequency in continuous mode). the peak current equals $I_{pk(min)}$.

When more output power is required, the switching frequency is kept constant on f_{min} (22.5 kHz). The I_{pk} level is increased to deliver the required power.

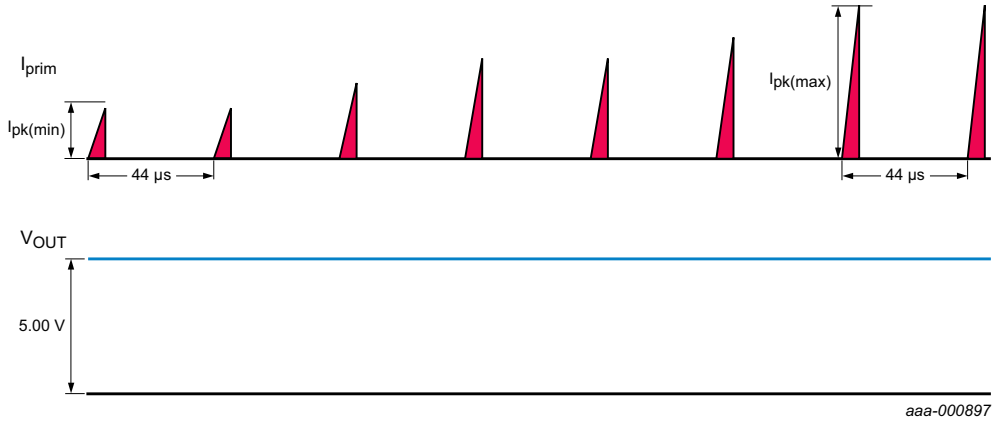


Fig 11. CVC mode with I_{pk} control

Remark: The on-time (t_{on}) increases with the amplitude of Ipk. This is not shown in simplified graphics like Figure 11.

In this mode, the peak voltage level on the SENSE pin increases from 120 mV to 530 mV.

P_{out} in the CVC mode is described with Equation 3:

$$P_{out} = 0.5 \times L_p \times I_{pk}^{2} \times f_{min} \times \eta \quad (3)$$

Where:

- I_{pk} = Varying from $I_{pk(min)}$ to $I_{pk(max)}$ (determined by V_{pk} on the SENSE pin)
- f_{min} = Minimum switching frequency in continuous mode (22.5 kHz)

When $I_{pk(max)}$ is reached, the IC enters the CVF mode.

6.2.3 CVF mode

The CVF mode (Constant Voltage Frequency regulation mode) takes over seamlessly where the CVC mode ends.

In this mode, the I_{pk} is kept constant on $I_{pk(max)}$. The frequency is increased to deliver the additional required power.

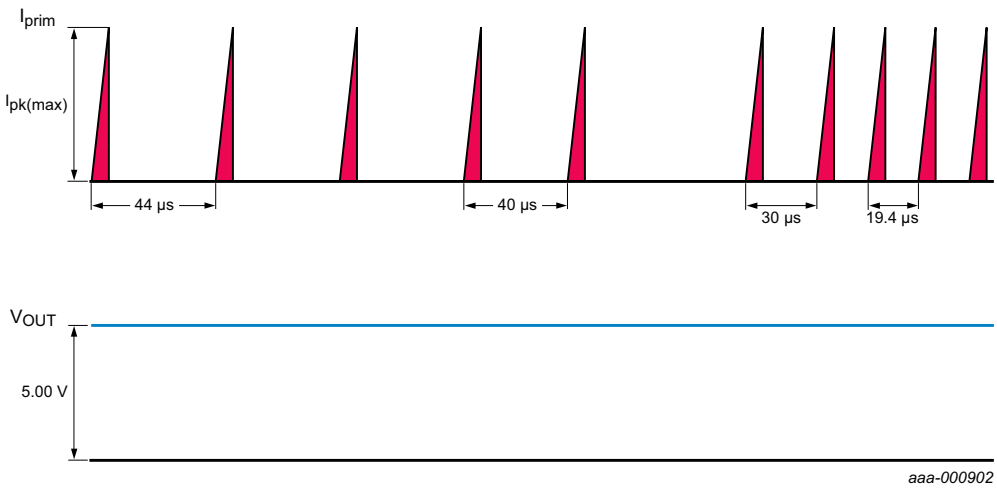


Fig 12. CVF mode with frequency regulation

The switching frequency is increased in this mode from f_{min} (22.5 kHz) to f_{max} (52 kHz).

The output power can be calculated with Equation 4:

$$P_{out} = 0.5 \times L_p \times I_{pk(max)}{}^2 \times f_{sw} \times \eta \quad (4)$$

Where:

- $I_{pk(max)}$ = Fixed maximum I_{pk} (V_{pk} = 530 mV on the SOURCE pin)
- f_{sw} = Switching frequency varies from f_{min} (22.5 kHz) to f_{max} (52 kHz)

The maximum output power is calculated using Equation 5:

$$P_{out(max)} = 0.5 \times L_p \times I_{pk(max)}{}^2 \times f_{max} \times \eta \quad (5)$$

This formula is useful for dimensioning the circuit. It is used in chapter 6.3 Transformer to calculate a practical circuit.

When the maximum power is exceeded, the IC switches to Constant Power mode.

6.2.4 Constant Power (CP) mode

The CP mode is the short transition between Constant Voltage mode and Constant Current mode.

In Constant Power mode the IC runs on maximum power (Equation 6).

$$P_{out(max)} = 0.5 \times L_p \times I_{pk(max)}{}^2 \times f_{max} \times \eta \quad (6)$$

The transition area is kept as small as possible.

6.2.5 CCF mode

To enter Constant Current mode, initially the maximum output power must be exceeded. This forces the IC to enter Constant Power mode. After that, the IC enters the CCF mode (Constant Current Frequency regulated mode).

When the load further increases, I_{out} is kept constant on $I_{out(max)}$, while V_{out} becomes the voltage, present over the load at $I_{out(max)}$.

It is the easiest to imagine the load as a resistive load. Increasing the load means decreasing the load resistance. A linear decreasing load resistance leads to a linear decrease of V_{out} over the load resistance at constant current $I_{out(max)}$.

To regulate to a fixed value $I_{out(max)}$, I_{pk} is kept constant and f_{sw} is reduced in CCF mode.

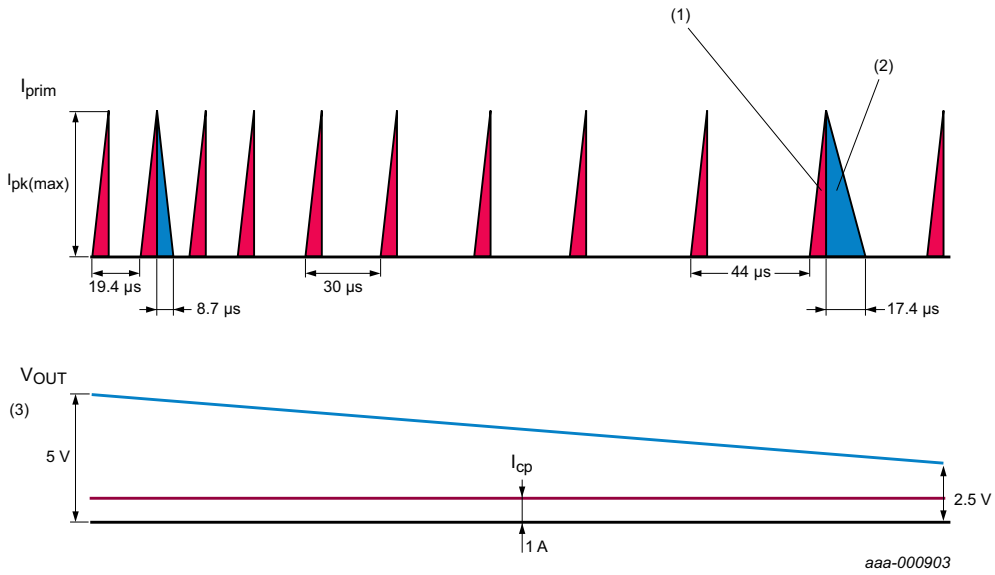


Fig 13. CCF mode regulation by frequency

The output power formula is the same as for CVF mode:

$$P_{out} = 0.5 \times L_p \times I_{pk(max)}{}^2 \times f_{sw} \times \eta \quad (7)$$

However, now f_{sw} is used to keep I_{out} constant, while V_{out} becomes the voltage over the load at $I_{out(max)}$.

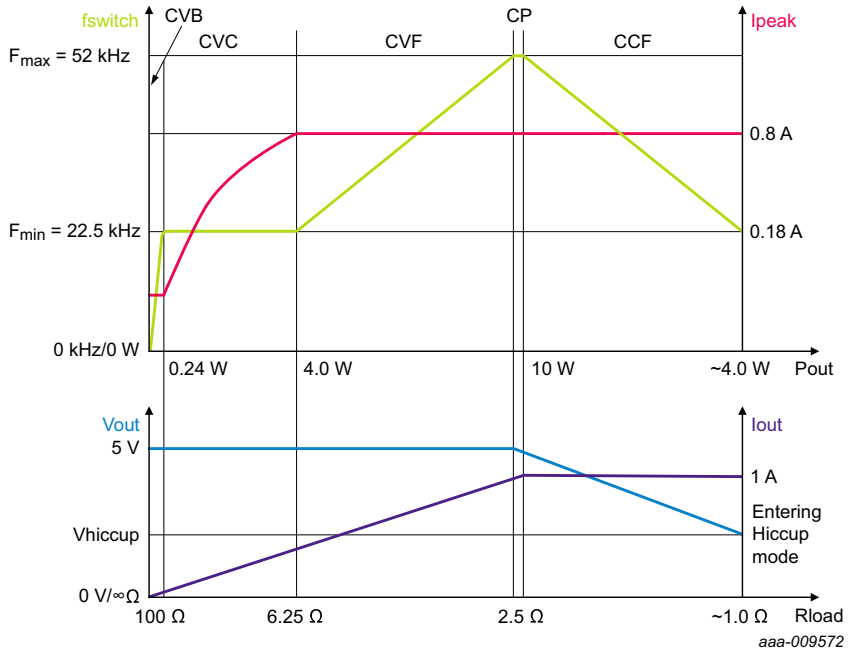
The switching frequency (f_{sw}) drops from f_{max} (52 kHz) to f_{min} (22.5 kHz).

Remark: The transition from CVF mode to CP mode to CCF mode is seamless.

When the output voltage drops to below the $V_{out(hiccup)}$ level for longer than 20.9 ms ($t_{blank(hiccup)}$), the overload protection becomes active. The IC stops switching and attemps to restart. As long as the overload condition is present the IC makes repetitive restart attempts. When the overload is removed, the IC restarts and resumes normal operation. See Section 6.12.6 for a detailed description of the hiccup mode protection.

6.2.6 Overview control modes

Figure 14 shows the control modes.



CVB = Constant voltage with burst mode

CVC = Constant voltage with current mode

CVF = Constant voltage with frequency mode

CP = Constant Power

CCF = Constant current with frequency mode

Hiccup mode: When below $V_{th(hiccup)}$ the IC restarts

Fig 14. Overview control modes

On the left V_{out} is kept constant, while on the right I_{out} is kept constant until V_{out} reaches the $V_{th(hiccup)}$ level.

6.3 Emitter drive NPN switch

The TEA1720 uses an emitter drive to control the external NPN switch. The advantages of the emitter drive are:

- Fast switch-on of the NPN switch
- Guaranteed switch-off of the NPN switch
- The reverse base current that is a result of the NPN BJT switching off is used to charge the VCC capacitor, preventing excessive switching losses

6.3.1 Emitter drive switch-on

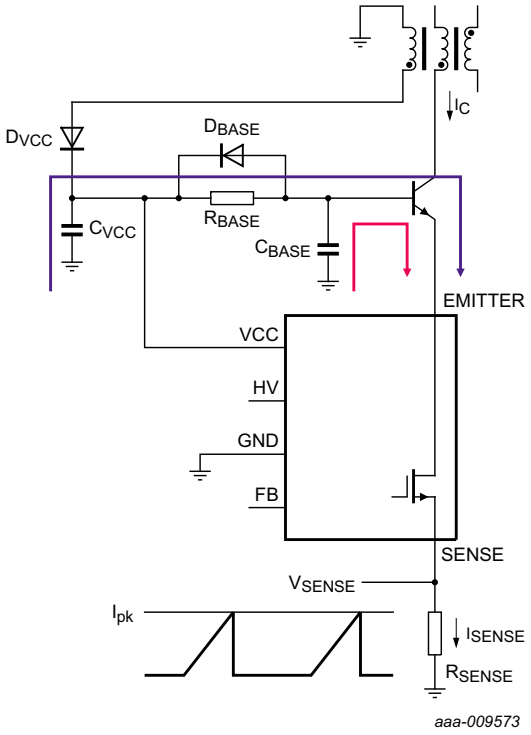


Fig 15. Emitter drive switch-on

When the internal MOSFET of the TEA1720 switches on, the emitter of the NPN is pulled low. The charge of the injection boost capacitor C_{BASE} is transferred directly to the base, ensuring an immediate switch-on of the NPN (NXP patent, patent pending). The sustaining base drive is delivered by capacitor C_{VCC} through R_{BASE}.

6.3.2 Emitter drive switch-off

When the NPN switch is on, the collector current increases linearly. The collector current and the base current are summed up. The resulting current exits through the emitter. The current flows from the emitter via the internal MOSFET through R_{SENSE}. Measuring the voltage level across R_{SENSE} (V_{pk}) determines the moment of switch-off. To compensate for the base current, a constant offset of 60 mV is subtracted from the measured level. This offset is equal to 12 % of the peak voltage for maximum I_{pk} (530 mV).

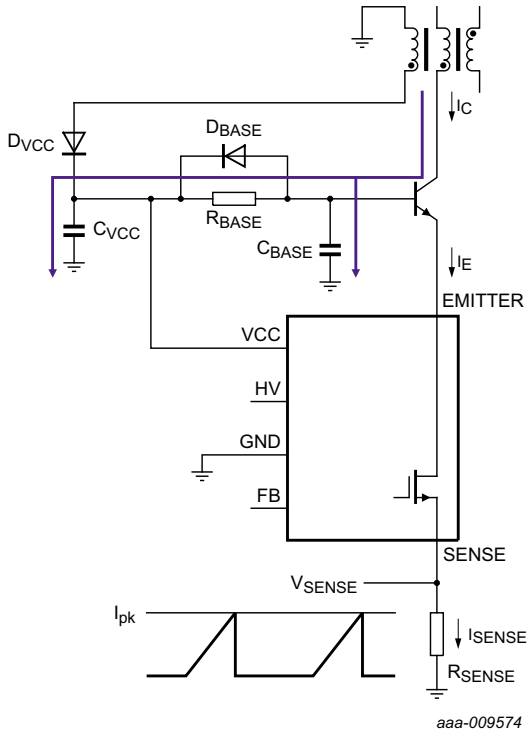


Fig 16. Emitter drive switch-off

When the V_{pk} level on the SENSE pin is reached, the internal MOSFET is switched off. The emitter current flow is blocked and the collector current exits through the base. The (negative) base current drains off the charge built-up in the collector. Once all charge is removed, it switches off the NPN. At the same time the negative base current charges capacitor C_{BASE} and capacitor C_{VCC} (via diode D_{BASE}) recovering part of the energy, involved in the base drive during on-time. The switch-off time is often called storage time, because it is the time required to drain off the stored charge, built-up in the collector region.

During the storage time, the collector current still continues to increase. The final collector peak current is therefore higher than the current measured at the SENSE pin at the moment of switch-off.

6.3.3 Waveforms

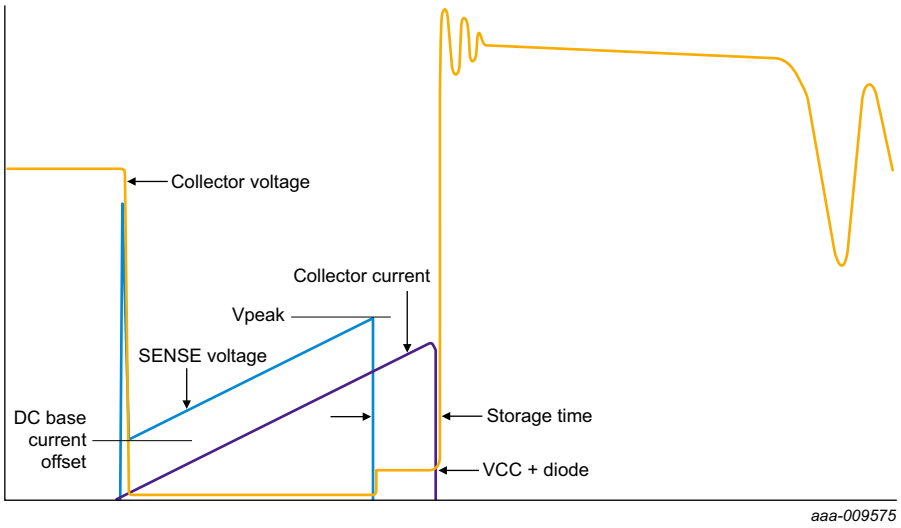


Fig 17. Waveforms emitter switching

Figure 17 shows the waveforms of the SENSE pin voltage, the collector current, and the collector voltage. At switch-on, the collector voltage drops to almost zero. The collector current starts to increase from zero. The initial charge injection provided by capacitor C_{BASE} is clearly visible in the SENSE pin voltage. After the spike, the SENSE pin voltage starts with a DC offset due to the base current injected via resistor R_{BASE}. From there the SENSE voltage follows the increasing collector current and increases more or less linearly.

When the voltage on the SENSE pin reaches V_{pk}, the internal MOSFET is switched off. The voltage on the SENSE pin immediately falls back to zero. The collector current continues but flows through the base, charging capacitor C_{BASE} and C_{VCC}. The collector voltage increases immediately to V_{CC} (+ voltage drop over diode D_{BASE}).

When all charge in the collector is removed, the NPN switches off. The collector current decreases to zero and the collector voltage increases for the start of the secondary stroke.

During the time the charge of the collector is drained off (storage time), the collector current continues to increase.

Remark: The storage time is not fixed. It changes roughly with a factor 1.7 from the high mains (264 V) to the low mains (85 V). The higher the mains voltage, the shorter the storage time.

6.3.4 Built-in compensations for emitter drive

The voltage, measured at resistor R_{SENSE}, does not reflect the peak collector current exactly. The actual power, however, is related to this peak collector current.

The TEA1720 comprises the following compensations for a controlled drive:

- DC offset compensation on the SENSE pin to compensate for the DC base current
- V_{in} compensation for V_{pk}, compensating for the change in storage time

6.3.4.1 DC offset compensation

The implementation is quite straight forward. A fixed offset of 60 mV is deducted from the level, measured on the SENSE pin. This offset is optimized for an NPN transistor with a h_{FE} of 9 to 10. Many low-power NPN transistors that are commonly used fall into this category.

6.3.4.2 V_{in} compensation

The collector current continues to increase during storage time. The final peak collector current is depending on:

- The steepness of the collector current, which is related to the rectified V_{in} (AC)
- The storage time, which is also related to the rectified V_{in} (AC)

Table 3 shows typical values for the storage time variation versus input voltage.

Table 3. Storage time BUJ100 at 0.8 A (peak)

Input voltage (V (RMS/AC))	85	264
Storage time (μs)	600	360

To cope with the variation, the peak collector current due to the variation of steepness of the collector current, and the storage time versus input voltage, V_{pk} is adapted in accordance with the input voltage.

To sense the input voltage, the level on the FB pin is measured during the primary stroke. This level is proportional to the input voltage.

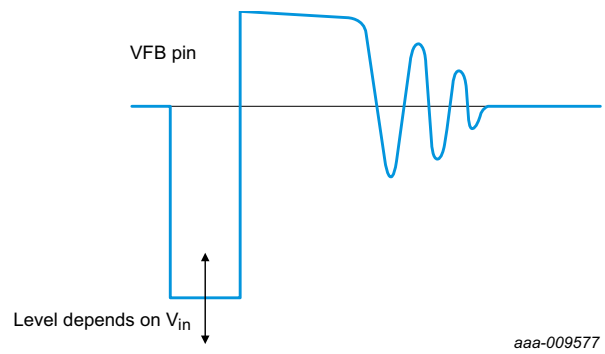
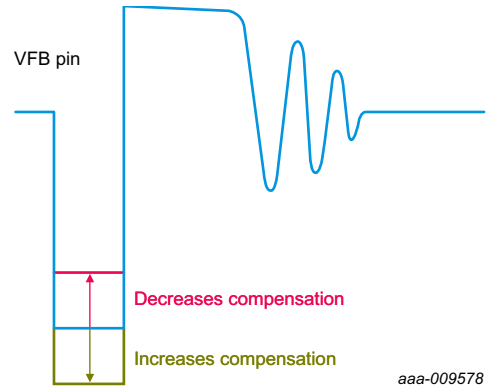


Fig 18. Sensing V_{in} on the FB pin

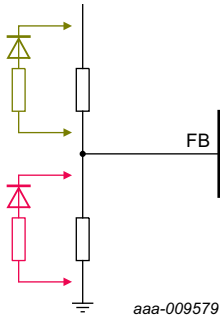
The V_{in} compensation enables the limiting of the variation of the maximum output power for all input voltages.

The built-in V_{in} compensation is designed for typical high-voltage low-power NPN transistors like the BUJ100 from NXP Semiconductors.

If NPN transistors are used with major deviations in h_{FE} and/or storage time, it is possible to adapt the V_{in} compensation externally.



a. Waveform



b. Schematic

Fig 19. Adapting V_{in} compensation externally

During primary stroke, the measured level on the FB pin can be tuned by adding a resistor in series with a diode parallel to one of the FB sense resistors.

Placing the circuit to ground in parallel with the divider resistor, decreases the V_{in} compensation, because the circuit is parallel to ground for negative voltages on the auxiliary winding, reducing the measured level on the FB pin.

Placing the circuit in parallel with the divider resistor from the FB pin to the auxiliary winding increases the V_{in} compensation because the circuit reduces the impedance of the top resistor for negative voltages.

6.3.5 Base drive dimensioning

Correct dimensioning of the NPN transistor base drive is vital for proper operation of the application. The components that are dimensioned are resistor R_{BASE} and capacitor C_{BASE}.

Aspects that play a critical role in the dimensioning process are:

- The peak collector current (I_{pk})

  Equals the peak current in the primary inductance of the transformer.
- The AC input voltage level

  The mains voltage that is supplied to the D1 to D4 rectifier bridge.
- The (quasi DC) voltage level that supplies the base current for the BJT (Q1)

  This voltage is referred to as the base drive voltage. In the diagram of Figure 16 it is the C_{VCC}//C_{BASE} voltage that is also used to supply the V_{CC} for the TEA1720A IC, so in our example the base drive voltage is V_{CC}.
- The current gain (h_{FE}) of the BJT (Q1)

  Especially the current gain at I_{pk} is important.
- The storage time (t_s) of the BJT (Q1)

6.3.5.1 Initial base drive dimensioning - the base resistor

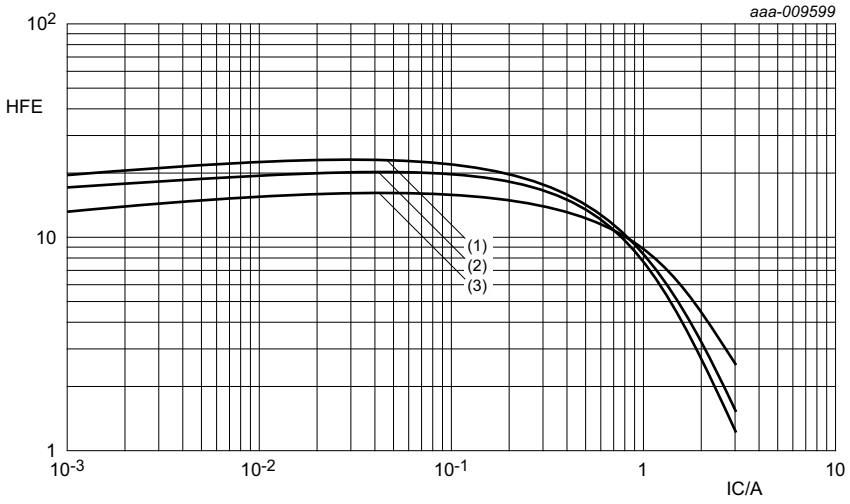
For initial dimensioning of the base drive resistor, the following information is required:

- The peak current in the primary winding of the transformer (I_{pk})
- The h_{FE} of the BJT at the peak current (I_{pk})
- The base drive voltage (V_{CC})

The peak primary winding current (I_{pk}) results from $V_{ref(pk)high}$ (typically 0.53 V) and the sense resistor value (R_{sense}).

$$I_{pk} = \frac{V_{ref(pk)high}}{R_{sense}} \quad (8)$$

An initial estimate for the BJT h_{FE} is read from the data sheet of the transistor used.



V_{CE} = 1 V

(1) +125 °C

(2) +25 °C

(3) −40 °C

Fig 20. Typical DC current gain ($h_{FE} = f(I_c)$; parameter V_{CE})

In a 10 W to 12 W flyback SMPS application, the peak primary winding current is usually programmed to be between 700 mA and 800 mA. At that current level the h_{FE} for a BUJ100 transistor is approximately 10.

In the application (see Figure 16) the auxiliary winding of the transformer generates the voltage (V_{CC}) for the BJT base drive. It equals the TEA1720A V_{CC} voltage. When a 'perfect transformer' is used, V_{CC} is clearly defined and is constant with the AC input voltage and the output power as long as the application is operating in constant voltage (CV) mode.

In reality, depending on the quality of the transformer (coupling between secondary and auxiliary winding), the generated V_{CC} voltage varies with the output power/output voltage produced by the flyback SMPS application. Furthermore, the output voltage also varies with the AC input voltage (mains voltage) the SMPS is connected to.

To calculate the initial value for R_{BASE}, an estimated value for the base-emitter voltage of the BJT is required under the condition that the BJT is on and saturated. Normally, that V_{BE} value is between 0.7 V and 1.0 V.

$$R_{BASE} = \frac{V_{CC} - V_{ref(pk)high} - V_{BE}}{I_{pk}} \cdot h_{FE} \quad (9)$$

Although it is not very likely that this initial dimensioning of the base drive resistor is fully optimal, it does result in a perfectly safe starting point for further optimization (see Section 6.3.5.2).

Example:

- I_{pk} = 800 mA
- h_{FE} = 10
- V_{CC} = 17.5 V
- $V_{ref(pk)high}$ = 0.53 V
- V_{BE} = 0.95 V

$$R_{BASE} = \frac{V_{CC} - V_{ref(pk)high} - V_{BE}}{I_{pk}} \cdot h_{FE} = \frac{17.5 - 0.53 - 0.95}{0.8} \cdot 10 \approx 200\ \Omega$$

6.3.5.2 Initial base drive dimensioning; the base capacitor

The base capacitor (C_{BASE}) delivers a charge carrier injection boost into the BJT BE-junction at the start of the primary stroke. This injection helps the BJT to reach an acceptably low $V_{CE(sat)}$ at the end of the primary stroke without requiring a high stationary injection that must be delivered through the base resistor (and would cause additional ohmic losses in the base resistor).

A low capacitor value has no significant contribution to charge carrier injection and therefore does not have a positive effect on the flyback SMPS operation. A very high base capacitor value results in a tremendous initial charge injection which can result in overdriving the BJT base, with corresponding increase of the switching losses.

As an initial value for C_{BASE}, we use a capacitor that can store all of the charge that is recovered from the BJT collector-base junction at the time of switch-off. The charge must be stored in the C_{BASE} capacitor at the V_{CC} level. This results in the following initial value for C_{BASE}:

$$C_{BASE} = \frac{I_{pk} \cdot t_s}{V_{CC}} \quad (10)$$

Unfortunately, I_{pk}, t_s and V_{CC} substantially vary depending on the operating conditions of the flyback SMPS. An appropriate C_{BASE} value for full load operation, can be (much) too large when the SMPS delivers low-power or no power. The result, higher/unacceptable losses in low load or a power consumption that is too high in a no-load condition. Therefore the C_{BASE} capacitor value is a subject for careful optimization (see Section 6.3.5.3).

For four relevant operating conditions we determine I_{pk}, t_s and V_{CC}. From those values we can calculate the optimum C_{BASE} for that condition (see Table 4).

Table 4. Suggested C_{BASE} values depending on the operating condition

Mains (V (AC))	Load	I_{pk} (mA)	t_s (ns)	V_{CC} (V)	C_{BASE} (nF)[1]
115	full load	650	330	20	10.7
115	no-load	150	250	12	3.1
230	full load	600	220	26	5.1
230	no-load	120	160	12	1.6

[1] Suggested initial values for CBASE are dependent on the operating condition.

As can be seen from Table 4 the suggested values for the C_{BASE} capacitor differ significantly depending on the operating condition of the flyback SMPS. A good starting point for a C_{BASE} capacitor is to take the logarithmic average of the suggested capacitance values belonging to all relevant operating conditions. If we qualify all the operating conditions in Table 4 as relevant, then the initial C_{BASE} value is:

$$C_{BASE(init)} = exp\left(\frac{1}{n} \cdot \sum_{i=1}^{n} 1n(C_{BASE_{init}})\right) \approx 4.1\ nF \quad (11)$$

A practical choice to start with is 3.9 nF.

6.3.5.3 Base drive dimensioning optimization

In the optimization process an attempt is made to achieve one general objective: Optimum overall efficiency of the flyback converter. However, while trying to realize that objective we have to take into account a number of limiting constraints for all other possible operating conditions:

- Keep the no-load power consumption of the flyback converter below a customer specified maximum value (for example, 20 mW or < 30 mW to fulfill Energy Star level 5)
- Keep the CV mode operation within the boundaries of 4.75 V and 5.25 V
- Keep the temperature of the BJT below a customer specified value (for example < 90 ° at room temperature at minimal input voltage and maximum load
- Keep the CC mode operation within the ±12 % variation limits
- Keep the conducted and radiated EMI below the levels as defined in CISPR 55022.
- Especially the variation of (ambient) temperature can be a severe constraint for proper operation

We must also pay attention to other aspects in the flyback converter application. However, the influence the base drive dimensioning has on these is negligible. For example, the maximum secondary diode temperature and the flyback transformer temperature must be below a customer specified maximum value (for example < 85° at room temperature at minimum input voltage and maximum load). But the base drive has no direct influence on that. These aspects must be considered in another phase of the flyback converter dimensioning process.

The optimization process

The base drive optimization process is time-consuming. Performance assessment sessions are required for a matrix of R_{BASE}/C_{BASE} values.

Performance assessment session

Basically, one performance assessment session (for one combination of R_{BASE} and C_{BASE}) consists of:

1. Measurement of the efficiency in the following (4 × 4) matrix:
   - At minimum mains (85 V (AC)/60 Hz), low mains (115 V (AC)/60 Hz), high mains (230 V (AC)/50 Hz), and maximum mains (265 V (AC)/50 Hz)
   - At 25 % load, 50 % load, 75 % load, and 100 % load
2. Measurement of no-load power consumption under the following conditions:
   - At minimum mains (85 V (AC)/60 Hz), low mains (115 V (AC)/60 Hz), high mains (230 V (AC)/50 Hz), and maximum mains (265 V (AC)/50 Hz)
3. Measurement of the output voltage in the following (4 × 5) matrix:
   - At minimum mains (85 V (AC)/60 Hz), low mains (115 V (AC)/60 Hz), high mains (230 V (AC)/50 Hz), and maximum mains (265 V (AC)/50 Hz)
   - At 0 % load (no-load), 25 % load, 50 % load, 75 % load, 100 % load.
4. Measurement of the R_{BASE} temperature at load (100 % load) and the following AC input voltage conditions:
   - At minimum mains (85 V (AC)/60 Hz), low mains (115 V (AC)60 Hz), high mains (230 V (AC)/50 Hz), and maximum mains (265 V (AC)/50 Hz)
5. Measurement of the BJT temperature under full load (100 % load) and the following AC input voltage conditions:
   - At minimum mains (85 V (AC)/60 Hz), low mains (115 V (AC)/60 Hz), high mains (230 V (AC)/50 Hz), and maximum mains (265 V (AC)50 Hz)
6. Measurement of the output current (in CC mode) in the following (4 × 5) matrix:
   - At minimum mains (85 V (AC)/60 Hz), low mains (115 V (AC)/60 Hz), high mains (230 V (AC)/50 Hz), and maximum mains (265 V (AC), 50 Hz)
   - At 95 %, 90 %, 80 %, 70 %, and 60 % of the nominal rated (CV) output voltage
7. Evaluation of conducted and radiated EMI under relevant conditions
8. Verification of proper operation under relevant conditions (e.g. temperature range)

In applications where, for example, CC mode is not relevant or where EMI is not important, the respective corresponding measurements can be skipped.

Varying R_{BASE} and C_{BASE}; filling the performance assessment session matrix

Start with the performance assessment session where $R_{BASE} = R_{BASE(init)}$ and $C_{BASE} = C_{BASE(init)}$ (the middle value in the matrix).

Table 5. Performance assessment session matrix

room for extension	.‴.‴.‴.‴.	.‴.‴.‴.‴.	.‴.‴.‴.‴.	room for extension
	$R_{BASE} = R_{BASE(nit)} * 0.67$ $C_{BASE} = C_{BASE(init)} * 0.5$	$R_{BASE} = R_{BASE(nit)} * 0.67$ $C_{BASE} = C_{BASE(init)} * 1.0$	$R_{BASE} = R_{BASE(nit)} * 0.67$ $C_{BASE} = C_{BASE(init)} * 2.0$	
	$R_{BASE} = R_{BASE(nit)} * 0.8$ $C_{BASE} = C_{BASE(init)} * 0.5$	$R_{BASE} = R_{BASE(nit)} * 0.8$ $C_{BASE} = C_{BASE(init)} * 1.0$	$R_{BASE} = R_{BASE(nit)} * 0.67$ $C_{BASE} = C_{BASE(init)} * 2.0$	
	$R_{BASE} = R_{BASE(nit)} * 1.0$ $C_{BASE} = C_{BASE(init)} * 0.5$	$R_{BASE} = R_{BASE(nit)} * 1.0$ $C_{BASE} = C_{BASE(init)} * 1.0$	$R_{BASE} = R_{BASE(nit)} * 1.0$ $C_{BASE} = C_{BASE(init)} * 2.0$	

Table 5. Performance assessment session matrix *...continued*

$R_{BASE} = R_{BASE(nit)} * 1.2$ $C_{BASE} = C_{BASE(init)} * 0.5$	$R_{BASE} = R_{BASE(nit)} * 1.2$ $C_{BASE} = C_{BASE(init)} * 1.0$	$R_{BASE} = R_{BASE(nit)} * 1.2$ $C_{BASE} = C_{BASE(init)} * 2.0$
$R_{BASE} = R_{BASE(nit)} * 1.5$ $C_{BASE} = C_{BASE(init)} * 0.5$	$R_{BASE} = R_{BASE(nit)} * 1.5$ $C_{BASE} = C_{BASE(init)} * 1.0$	$R_{BASE} = R_{BASE(nit)} * 1.5$ $C_{BASE} = C_{BASE(init)} * 2.0$
.....	.....	.....

Plot the tendency in the efficiency figures in a 3-dimensional graph (efficiency as a function of R_{BASE} and C_{BASE}). If the efficiency has not reached a maximum, extend the R_{BASE} range in steps of a factor ~1.2 (higher or lower) and/or the C_{BASE} range in steps of a factor of ~2 (higher or lower) until a maximum efficiency value is found.

Provided that there is no conflict with the constraints listed above, the optimum for the R_{BASE}/C_{BASE} combination is found. Fine-tuning of the R_{BASE}/C_{BASE} combination using finer variation steps is an option.

A word of caution - overdriving and underdriving

Overdriving the base oversaturates the BJT which usually results in (much) higher than necessary switching losses. It is inefficient but not immediately catastrophical.

On the other hand underdriving the base causes an undersaturated situation in the BJT which leads to a high VCE voltage drop during on-state and consequently (very) high conduction losses. Significant underdriving can rapidly lead to a thermally unstable situation and thermal runaway, destroying the BJT.

The maximum efficiency is achieved under so-called "lean driving" conditions. Lean driving conditions set the best balance between switching losses and conduction losses.

To be on the safe side, a BJT can be slightly overdriven, but preferably not underdriven. Underdriven BJTs are much more prone to failure.

Finally, there can be (application specific) constraints that can impose minimum or maximum value requirements on R_{BASE} and C_{BASE}.

6.3.5.4 Verification of R_{BASE} at low temperatures

After optimizing R_{BASE}, it is important to check the drive under all operating conditions. This requirement is the most critical at start-up at low temperatures.

Check the start-up of the application at the lowest V_{in} (AC) and at the lowest specified ambient temperature. The voltage at the SENSE pin must reach V_{pk} at start-up until V_{CC} reaches 8.5 V ($V_{CC(stop)}$).

This check can be done by disconnecting the diode (D_{VCC}) from the auxiliary winding to the VCC capacitor. After the VCC capacitor is charged to 17 V ($V_{CC(start)}$), switching starts and continues until V_{CC} reaches 8.5 V ($V_{CC(stop)}$) because the V_{CC} supply is not taken over by the auxiliary winding.

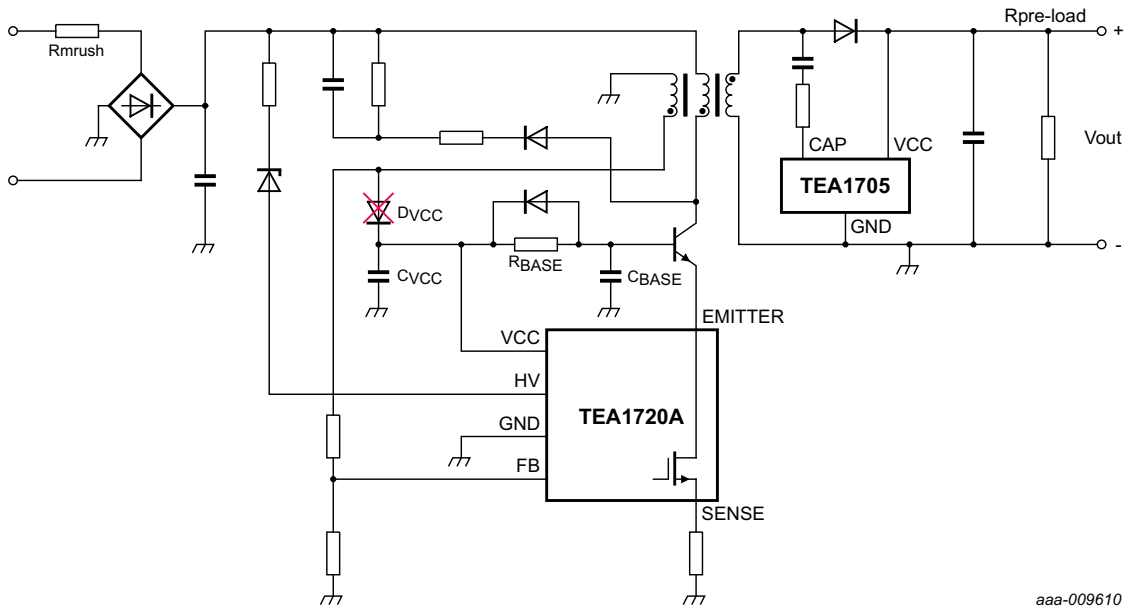
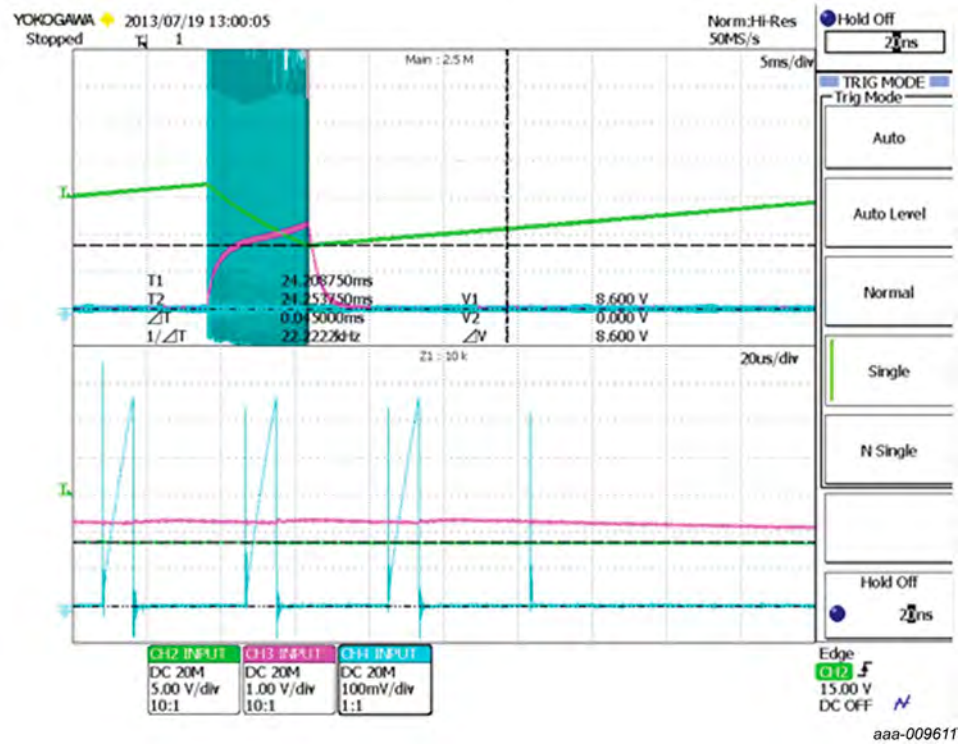


Fig 21. Setup for checking base current

Put the application in a temperature chamber and bring the temperature to the lowest ambient temperature specified.

Measure the voltage on the VCC and SENSE pins. Especially monitor the last strokes before V_{CC} reaches 8.5 V and switching stops. V_{pk} must be reached.



Green = V_{CC}

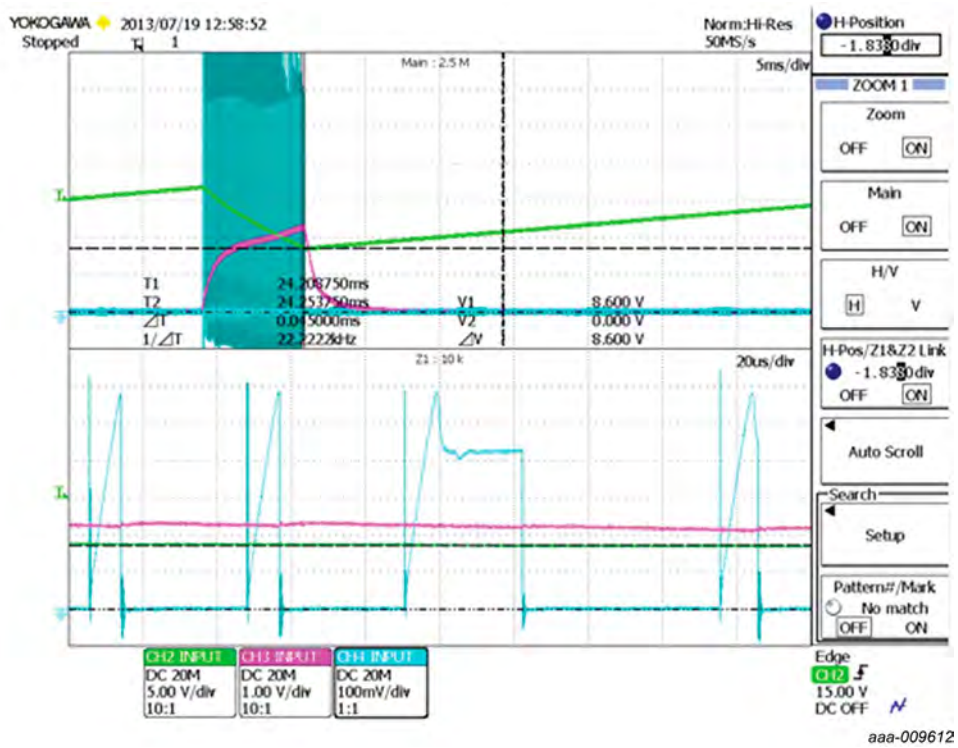
Purple = V_{out}

Blue = V_{sense}

Fig 22. Base current high enough

For checking the voltage on the SENSE pin, zoom in on the part where switching stops. It is clear the voltage at the SENSE pin remains correct until 8.5 V is reached ($V_{CC(stop)}$). The last stroke is ended as soon as $V_{CC(stop)}$ is reached.

Figure 23 shows an example of the waveform on the SENSE pin when V_{pk} is not reached.



Green = V_{CC}

Purple = V_{out}

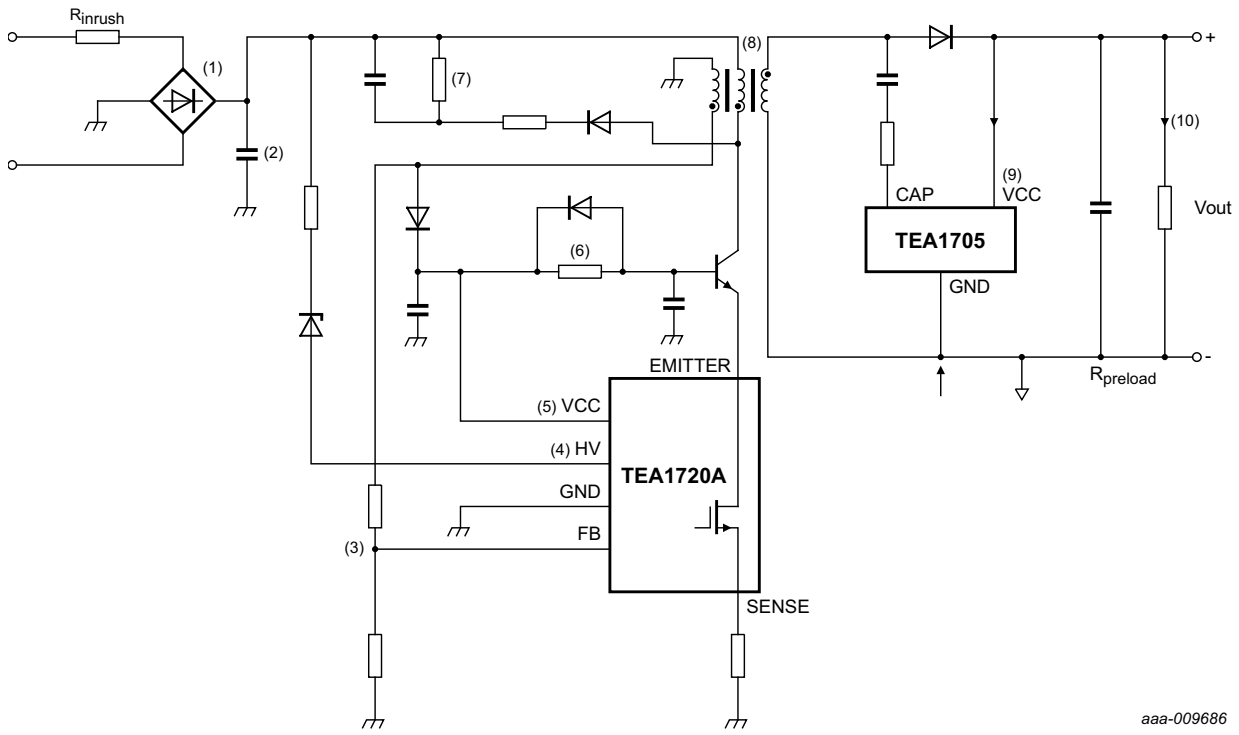
Blue = V_{sense}

Fig 23. Base current too low to reach V_{pk}

Zooming in on the last strokes before switching stops, V_{pk} is not reached in the last full stroke. The current keeps flowing until the maximum duty cycle is reached (75 %). R_{BASE} must be lowered to prevent that this condition occurs.

6.4 Total input power at no-load

The input power at no-load consists of several components. An overview is given below:



For a 10 W charger, the no load losses are:

(1) Leakage rectifier: 2 × 0.1 μA at 375 V = 0.1 mW

(2) Leakage mains electrolytic capacitors: 5 μA at 375 V = 2 mW (estimated)

(3) FB sensing resistive divider: Only dissipating during primary and secondary stroke = 0.1 mW

(4) Leakage HV current source: 1 μA at 375 V = 0.4 mW

(5) Supply current IC: 130 μA at 15 V = 2 mW

(6) Base drive losses = 4 mW

(7) Snubber losses = 2 mW

(8) The stored energy ($0.5 \times L_p \times I_{pk}^2$) is divided between the V_{CC} (basedrive + IC supply current) and the secondary load (transient detector and preload)

(9) Supply current transient detector: 0.1 mA at 5 V = 0.5 mW; influence on no-load power negligible; can be compensated by adapting the preload resistor value.

(10) Preload resistor: 3.6 kΩ; tuned to prevent V_{out} rises at maximum V_{in} (264 V (AC)); dissipation = 7.5 mW

Fig 24. Overview of no load losses

Adding up all numbers the result for a 10 W charger is:

$$P_{noload} = 0.1 + 2 + 0.1 + 0.4 + 2 + 4 + 0.5 + 7.5 = 18.6\ mW \quad (12)$$

For a 5 W charger, the P no-load is roughly half (< 10 mW). For a 12.5 W charger, the P no-load remains < 30 mW.

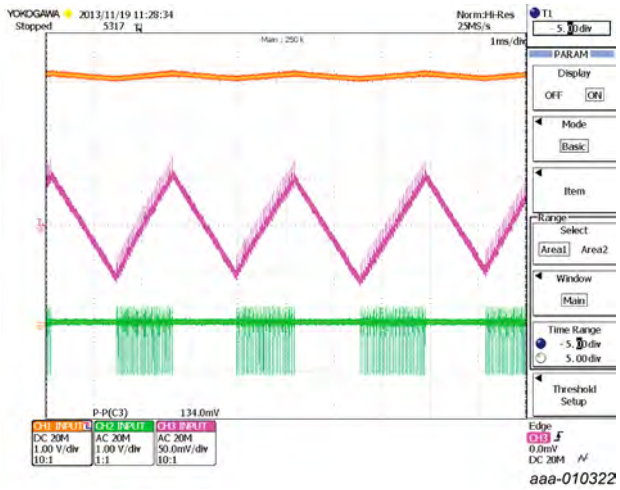
6.5 Value output capacitor, ripple, load step, transient controller

The value of the output capacitor is key in determining properties, like ripple and load step behavior.

6.5.1 Ripple

For minimal ripple at full load, use two capacitors with a low ESR, like aluminum polymer electrolytic capacitors, in parallel.

Due to the low burst frequency, ripple also occurs in burst mode. This ripple is highest when the duty cycle in burst mode is around 50 % which is 50 % switching including the recharging of the output capacitors and 50 % non-switching including the discharging of the output capacitors. Because the peak current is highest at the highest input voltage, the ripple is also highest at the maximum input voltage (V_{in}).



V_{in} (AC) = 264 V; I_{load} = 72 mA; $V_{out(ripple)}$ (peak-to-peak) = 134 mV
Orange = V_{out} (DC; 1 V/div)
Green = FB pin; indicating the switching of the controller
Purple = Ripple V_{out} enlarged (AC; 50 mV/div)

Fig 25. V_{out} ripple at 50 % switching in burst mode

Practical example

- For a 10 W charger, the load current at 264 V (AC)/50 % duty cycle in burst mode is 72 mA.
- f_{burst} = 400 Hz; t_{burst} = 2.5 ms, 50%; t_{burst} = t_{ch} = t_{dch} = 1.25 ms.
- Take two 470 µF output capacitors

The actual value of the output capacitors can be 80 %. So in practice the output capacitor value becomes: $C_{out} = 0.8 \times (2 \times 470\ \mu F) = 750\ \mu F$.

The discharge voltage (V_{dch}) during non-switching (which is equal to the charge voltage (V_{ch}) during switching) can be calculated with Equation 13.

$$V_{dch} = I_{load} \times \frac{t_{dch}}{C_{out}} = 0.072 \times \frac{0.00125}{750^{6}} = 120\ mV \quad (13)$$

With an additional 20 mV ripple, the resulting peak-to-peak ripple is 140 mV

Use the values in Table 6 when the ripple < 150 mV.

Table 6. C_{out} for peak-to-peak ripple <150 mV

f_{burst}	$P_{out(nom)}$	$C_{out(nom)}$
400 Hz	10 W	2 × 470 µF
400 Hz	5 W	2 × 270 µF

6.5.2 Load step without transient control

When a load step occurs while the TEA1720 is switching, the loop responds immediately and V_{out} remain within the USB 1.1 specification limits.

The situation is different when the load step occurs during the non-switching time in burst mode because the primary sensing concept is "blind" to what happens on the secondary side when the IC is in energy save mode between burst periods.

For load steps without transient controller, the USB 1.1 specification (see Section 8.1.1) is followed in most cases.

USB 1.1 requires that V_{out} remains above 4.1 V for a 0 A to 0.5 A load step.

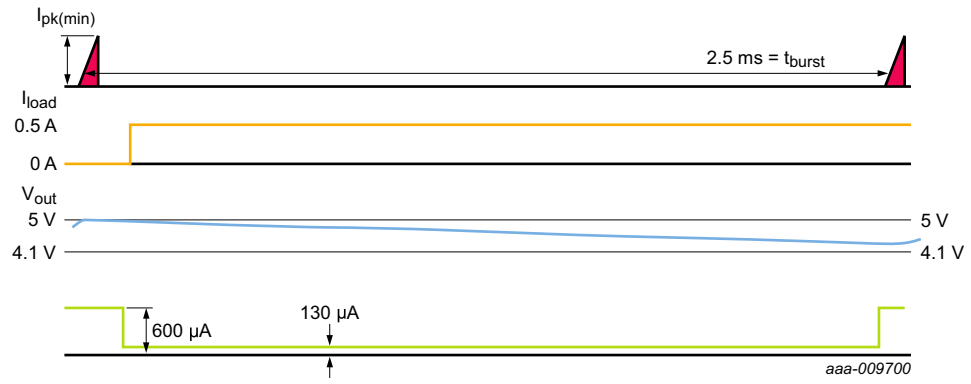


Fig 26. Load step without transient controller

The worst case is when the load step occurs as the IC enters energy save mode. The maximum time the capacitor has to maintain the output voltage is $1/f_{burst}$.

The capacitor value can be calculated with Equation 14:

$$C_{out} = \frac{I_{load}}{(f_{burst} \times V_{drop})} \quad (14)$$

Where:

- I_{load} is the current after load step
- V_{drop} is the output voltage (V_{out}) at the beginning of load step –4.1 V

Equation 14 clearly indicates the relation between the output capacitor (C_{out}) and the burst frequency (f_{burst}).

Example:

Due to the internal load line of 250 mV, V_{out} at no-load is at least 5.00 V. As a result, the voltage on the output capacitor can drop from 5.00 V to 4.10 V.

- V_{drop} = 0.9 V
- I_{load} = 0.5 A
- f_{burst} = 400 Hz

$$C_{out(min)} = \frac{0.5}{(400 \times 0.9)} = 1388 \times 10^{-6}$$

The result is the minimal required value for the capacitor (C_{out}). Most electrolytic capacitors have a 20 % tolerance on the low-side. Divide the calculated value by 0.8 to obtain the nominal value.

$$C_{out(nom)} = \frac{1388^{-6}}{0.8} = 1736^{-6} \quad (15)$$

This is one 1000 μF capacitor and one 820 μF capacitor in parallel (or two 820 μF capacitors in parallel at a maximum negative tolerance of −15 %.

Table 7 shows the results.

Table 7. C_{out} for USB 1.1 without transient controller

f_{burst}	$C_{out(nom)}$	Maximum negative tolerance
400 Hz	1000 μF + 820 μF	−20 %
400 Hz	2 × 820 μF	−15 %

Remark: The USB 1.1 specification specifies only one load step current (0 A to 0.5 A). It is not related to the available maximum output power.

6.5.3 Transient controller (TEA1705)

To improve the load step performance in burst mode, the transient controller TEA1705 can be added.

The TEA1705 is placed on secondary side. It monitors continuous V_{out} via the VCC pin. When V_{out} drops to below 4.9 V, when the TEA1720 is in burst mode and not switching (energy save mode), the TEA1705 generates a wake-up pulse via the transformer to trigger the TEA1720 to immediately start switching.

Using the TEA1705 in a 10 W charger with 2 × 470 μF output capacitor, the 0 A to 2 A load steps can be handled while V_{out} remains > 4.5 V.

6.5.3.1 Circuit diagram

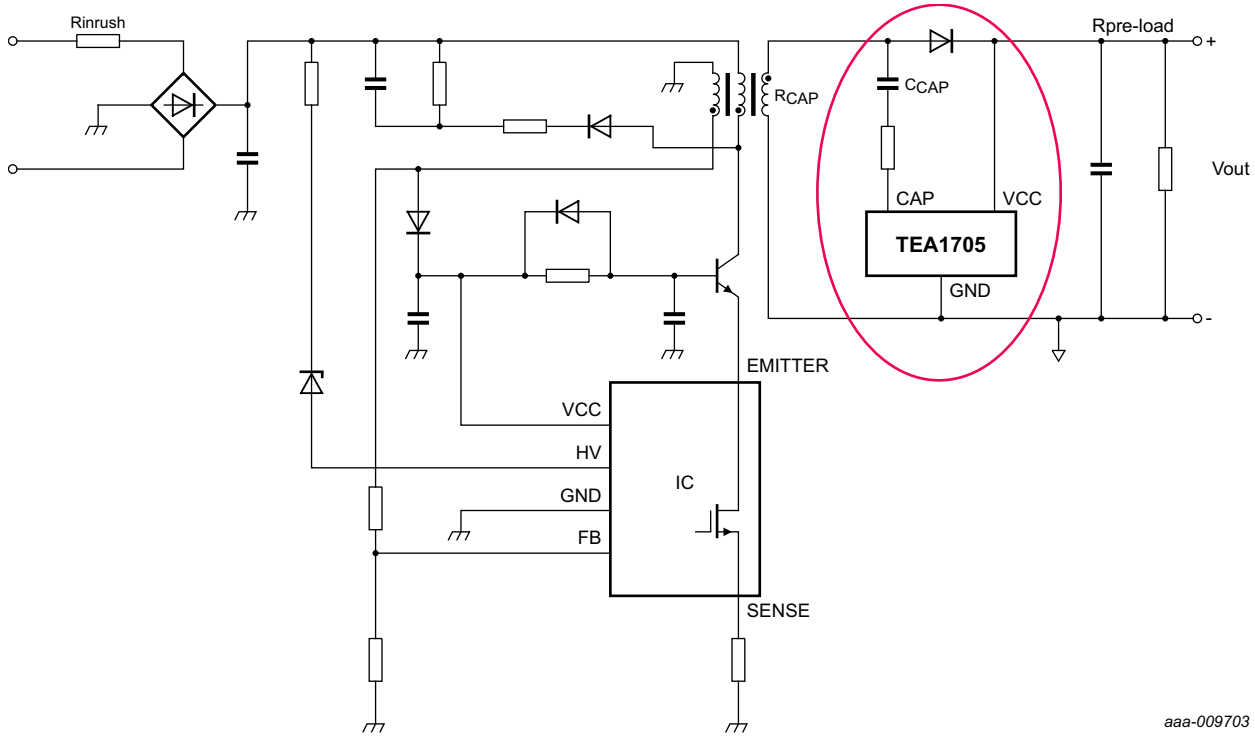


Fig 27. Schematic diagram showing TEA1705

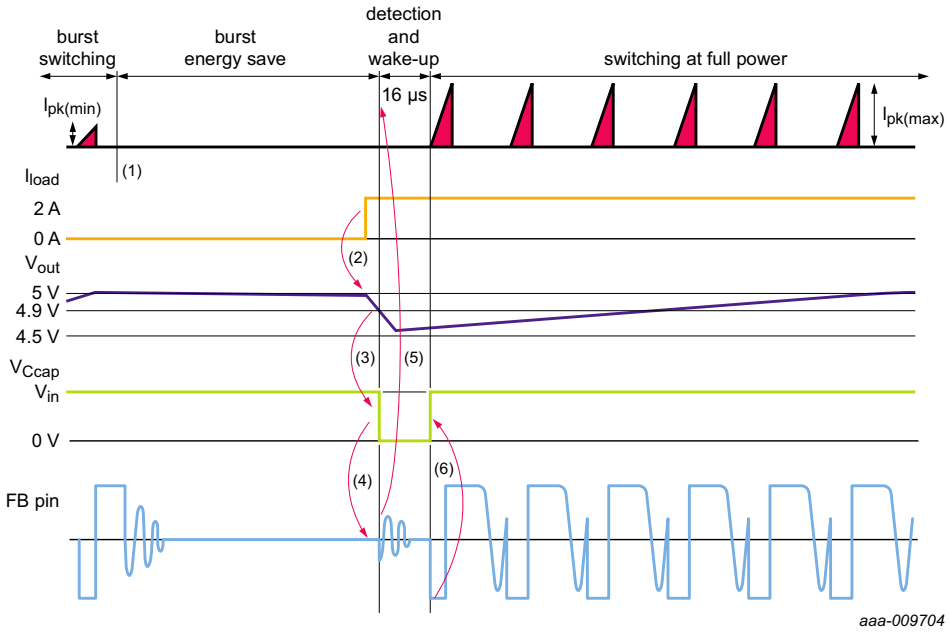
The VCC pin serves as supply pin and to monitor V_{out}. The supply current of the TEA1705 is only 100 μA. This current does not affect the no-load power. It can be compensated by adapting resistor $R_{PRELAOD}$ if required.

Only two additional components are required in the application, R_{CAP} and C_{CAP}. Typical values are:

- R_{CAP} = 4.7 Ω
- C_{CAP} = 47 nF

6.5.3.2 Transient controller mechanism

Figure 28 shows how the transient controller mechanism operates.



(1) The burst switching ends and the TEA1720 enters energy save mode. The transient detector on the FB pin is enabled. The TEA1705 detects that no switching occurs and becomes active after 70 µs.

(2) A load step of 0 A to 2 A occurs causing V_{out} to drop.

(3) When V_{out} reaches 4.9 V, the internal MOSFET between the capacitor C_{CAP} and GND switches on for 1.2 µs and discharges C_{CAP} over the secondary winding.

(4) The discharging of C_{CAP} causes ringing in the transformer windings and generates a wake-up pulse at the FB pin.

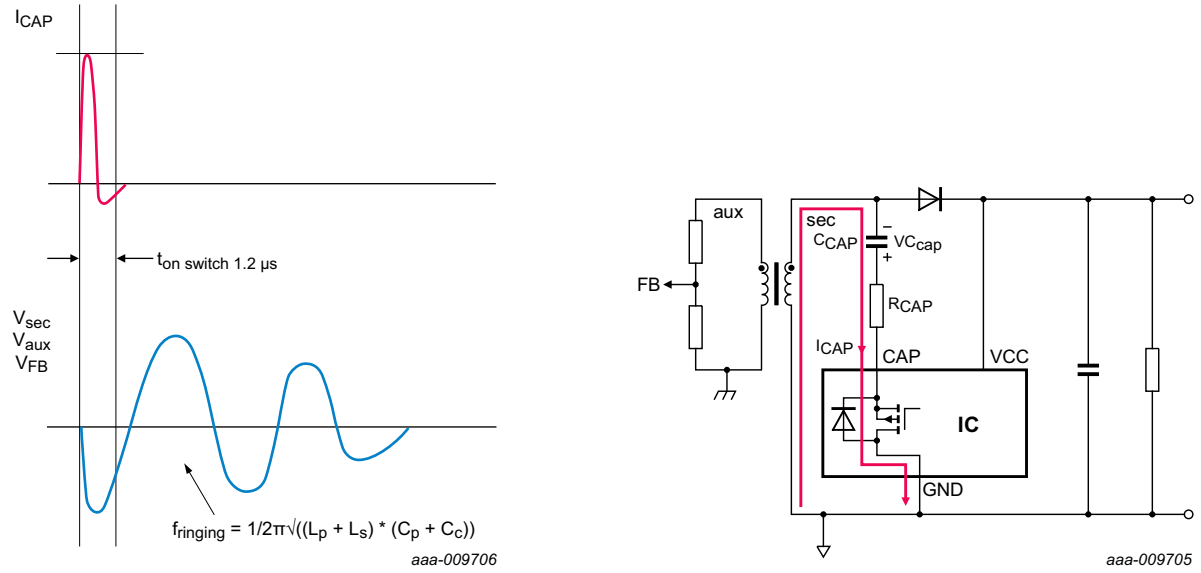
(5) The wake-up pulse is detected by the FB pin. The TEA1720 wakes up from energy save mode. After 16 µs switching starts at full power. V_{out} start to rise.

(6) During the first primary stroke, C_{CAP} recharges and is ready for the next load step.

Fig 28. Load step during burst with transient controller

6.5.3.3 TEA1705 generation wake-up pulse

Figure 29 shows the generation of the wake-up pulse.



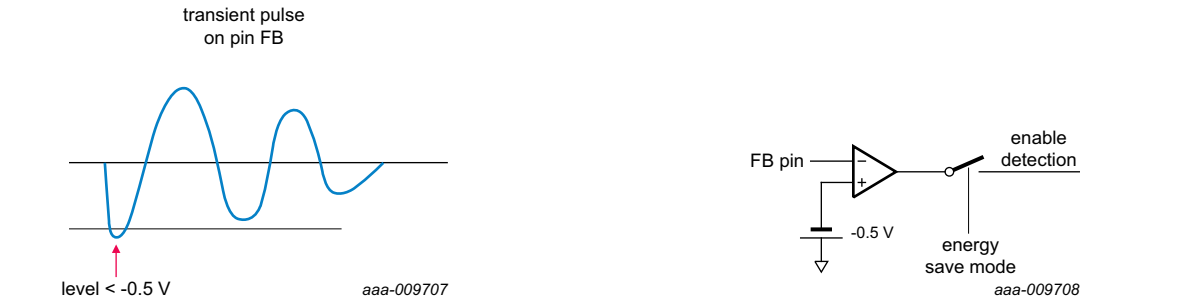
a. Waveform b. Schematic

Fig 29. Wake-up pulse generation, C_{CAP} discharge

When the internal MOSFET of the TEA1705 is on for 1.2 µs, C_{CAP} is discharged. The discharge causes a step response on the secondary winding (and all other windings). After the step the transformer starts a damped ringing with the same frequency and damping as after the secondary stroke.

6.5.3.4 TEA1720 transient detector

Figure 30 shows the detection of the wake-up pulse.



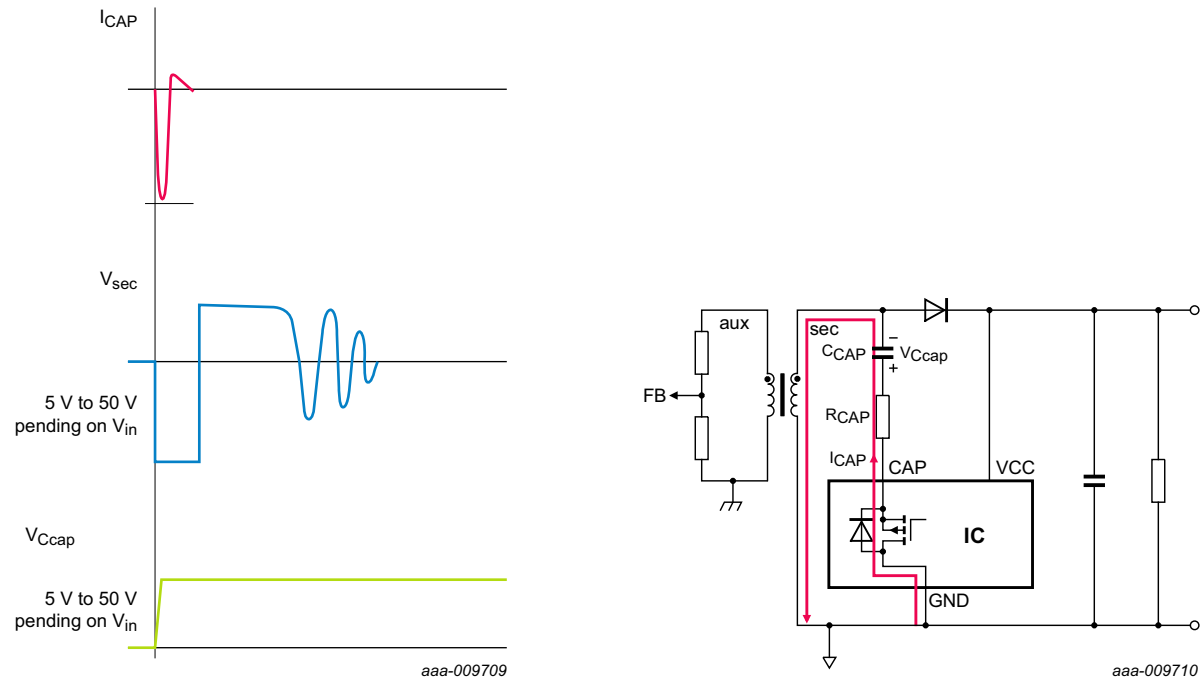
a. Waveform b. Schematic

Fig 30. TEA1720 transient detector

The transient detector in the TEA1720 is a comparator with a detection level of −0.5 V. To prevent false detection, the transient detector in the TEA1720 is only enabled during the energy save mode where no switching occurs and the level on the FB pin is 0 V.

6.5.3.5 TEA1705 charging C_{CAP}

Figure 31 shows the charging of CCAP.



a. Waveform

b. Schematic

Fig 31. Charging C_{CAP} during primary stroke

When switching starts, the voltage on the secondary winding is negative. This negative voltage charges C_{CAP} via the backgate diode of the TEA1705 internal MOSFET. R_{CAP} is added to limit the charge current to safe values (< 3 A).

The amplitude of the negative voltage is proportional to V_{in} (AC). The charge on C_{CAP} is always high enough, even at the lowest AC input voltage, when the values C_{CAP} = 47 nF and R_{CAP} = 4.7 Ω are used.

6.5.3.6 TEA1720 switching detector and wake-up pulse disable timer

To prevent unnecessary discharge of C_{CAP}, the TEA1705 also contains a switching detector (see Figure 32).

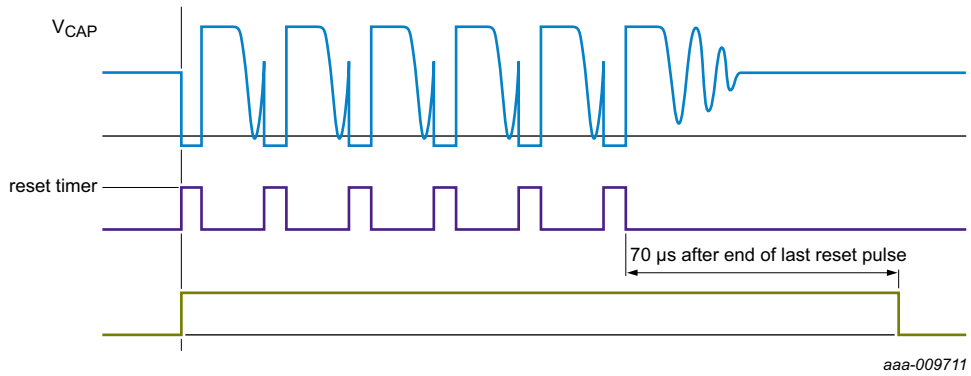


Fig 32. Switching detector with disable timer wake-up pulse

The switching detector monitors the voltage on the CAP pin. When an AC signal is present it detects the lowest level, which is during primary stroke.

The detection resets the internal 70 µs timer. As long as the timer is active (as long as switching occurs), the generation of the wake-up pulse is disabled. 70 µs after the last stroke detection the generation of wake-up pulses is enabled. Only when the TEA1720 enters energy save mode this condition occurs.

Remark: The TEA1705 can only generate a wake-up pulse and the TEA1720 can only detect a wake-up pulse during energy save mode.

6.5.3.7 TEA1705 no-load V_{out} protection

When V_{out} exceeds 5.9 V, the VCC pin of the TEA1705 starts to draw current (see Figure 33).

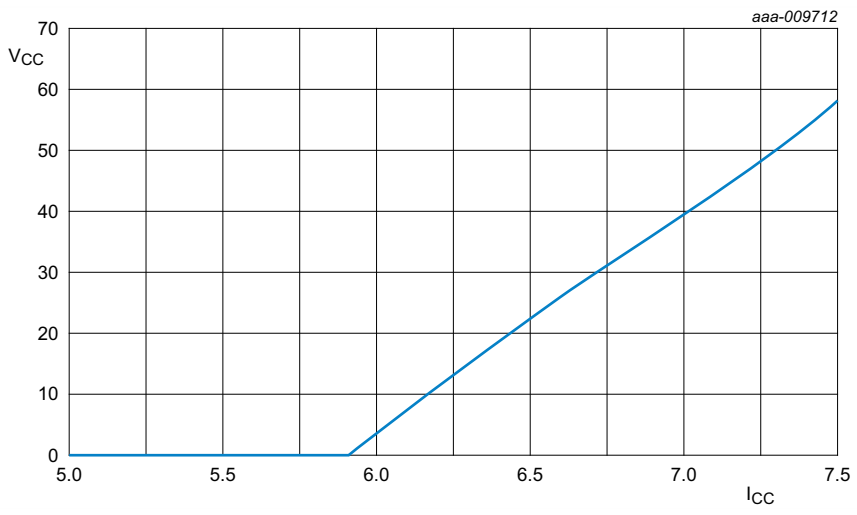


Fig 33. No-load V_{out} protection

The VCC current increases linearly from 0 mA at 5.9 V to 40 mA at 7.0 V. At 6.3 V, the current is 15 mA, which corresponds with a secondary load of 95 mW.

This protection prevents V_{out} rises above 6.3 V, causing leakage of the often used polymer output electrolytic capacitors with a 6.3 V rating when the preload resistor provides insufficient load or no preload resistor is mounted.

6.6 Feedback

In a primary sensed system, the output voltage is regulated by measuring the voltage of an auxiliary winding on primary side.

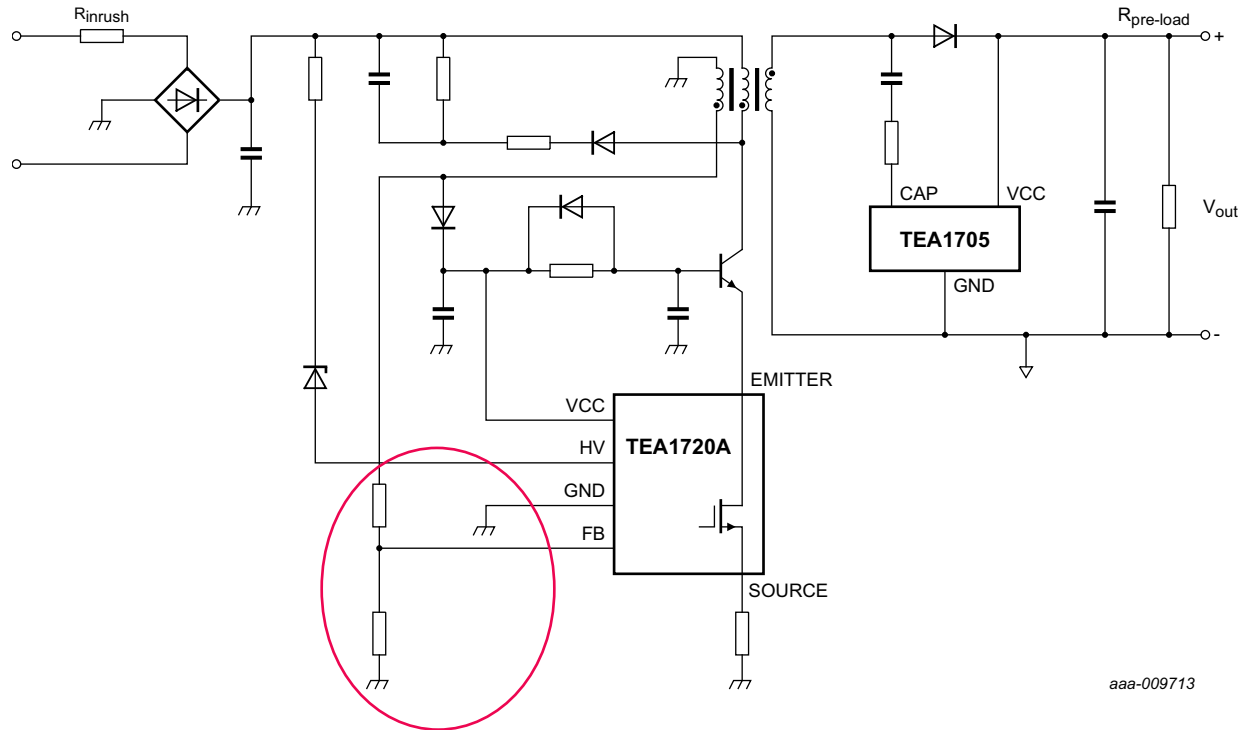
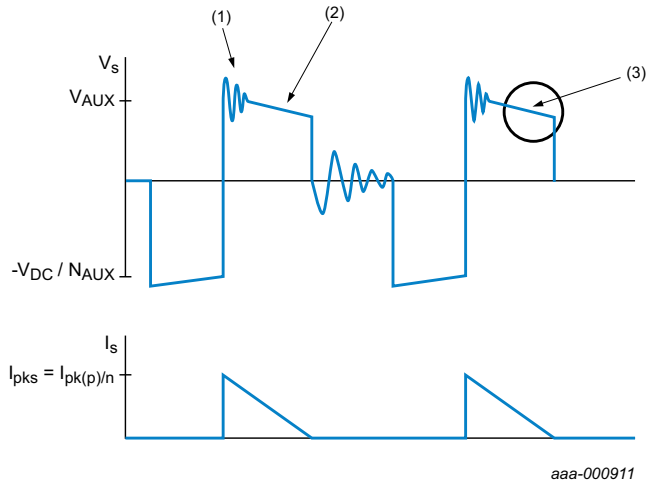


Fig 34. Feedback from auxiliary winding

For optimal matching of the auxiliary winding and the output voltage, couple the transformer auxiliary winding to the secondary winding tightly.

Due to the primary sensing concept, the secondary voltage is regulated before the secondary diode. Changes in voltage drop over the diode are not corrected and are reflected in the V_{out} level.

Figure 35 shows the waveform on the auxiliary winding.



(1) No accurate measurement possible during ringing.

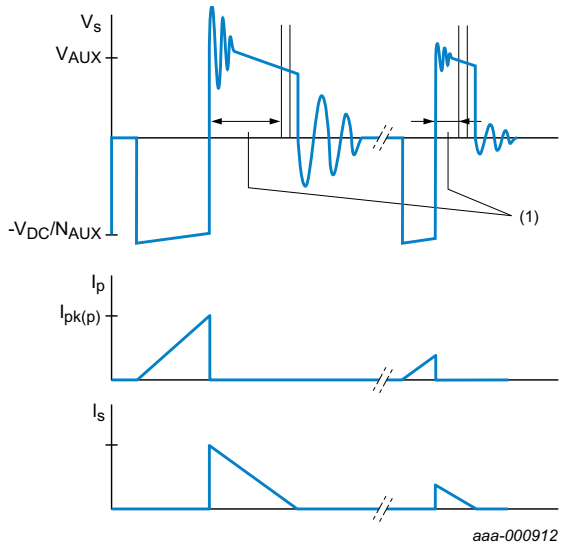
(2) Voltage drops due to decreasing voltage over the secondary diode with decreasing current.

(3) Measurements done towards the end of the secondary stroke at minimal secondary current to increase accuracy and avoid ringing.

Fig 35. Waveform auxiliary winding

V_{out} is measured during the secondary stroke. To increase the accuracy, V_{out} is sampled near the end of the secondary stroke. This timing minimizes the influence of the voltage drop over the secondary diode because the diode current is close to zero. It also minimizes errors because of ringing.

As the secondary stroke time varies with the value of I_{pk} (the higher I_{pk}, the longer the secondary stroke time), the sample time is adapted accordingly.



(1) To increase measurement accuracy, the position of the measurement pulse is adapted to the duration of the secondary current. A measurement is done near the end of the stroke where the secondary stroke is close to zero and ringing is minimal.

Fig 36. Adaptive sample time

Configure the resistive divider on the FB pin to deliver 2.5 V at the FB pin near the end of the secondary stroke (burst mode). Take into account that the voltage near the end of the secondary winding is $V_{out} + V_{diode}$.

6.7 Demagnetization protection

The signal of the auxiliary winding on the FB pin is also used for demagnetization protection. That is, to determine if the secondary stroke has ended and all stored energy in the transformer is transferred to secondary side.

To release the demagnetization protection, the voltage on the FB pin must drop to < 50 mV after the secondary stroke has started. When no demagnetization is detected, the next primary stroke is prohibited until demagnetization detection is true. This condition ensures discontinuous operation.

6.8 Supply from auxiliary winding

The IC and the base drive are supplied from an auxiliary winding. It is possible to use the feedback auxiliary winding or a separate winding.

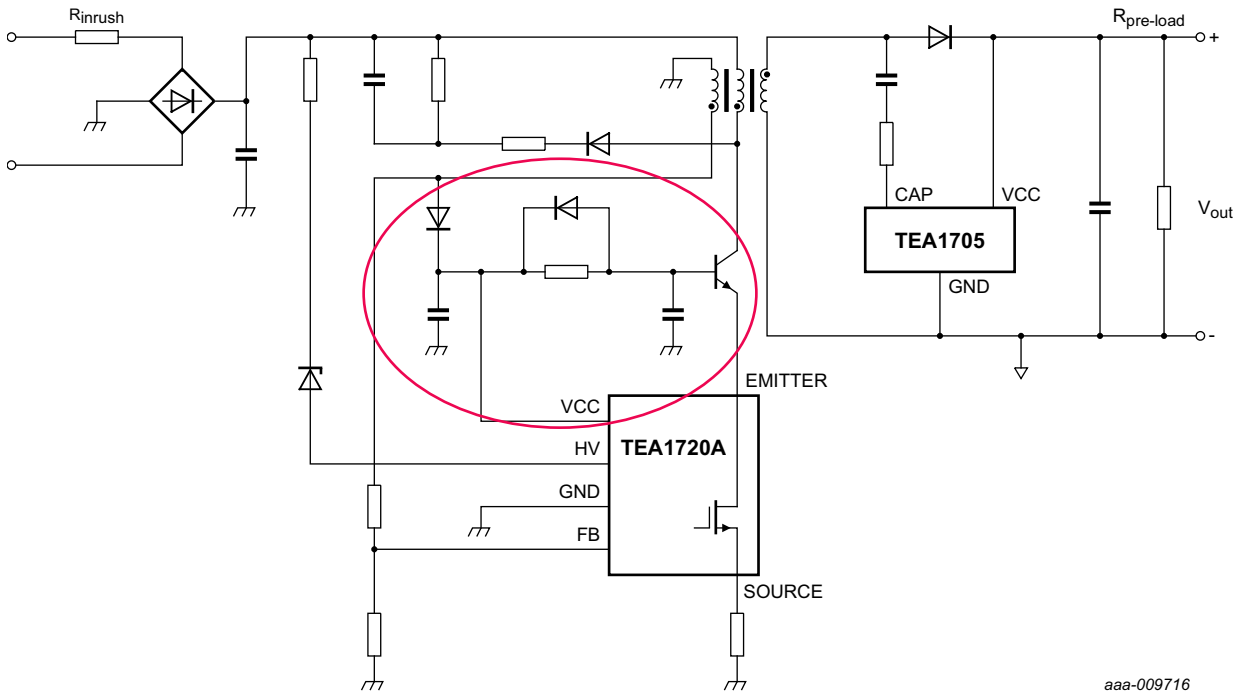
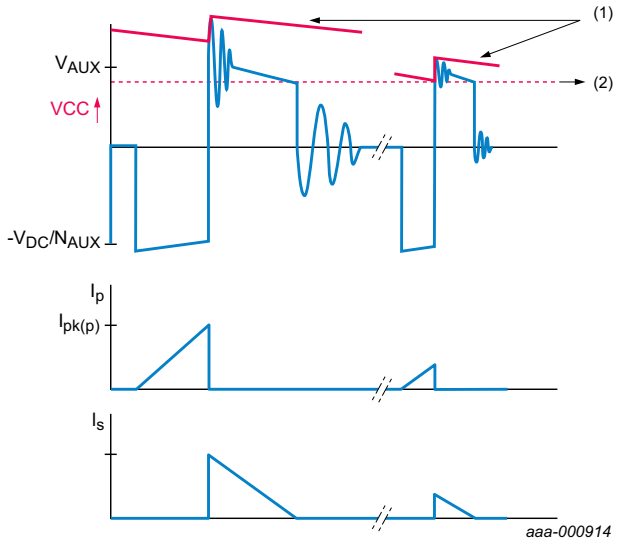


Fig 37. Supply from auxiliary winding

When designing the auxiliary winding, consider the waveforms on the winding as shown in Figure 38.



(1) Actual V_{CC}, resulting from peak rectification of the ringing

(2) V_{CC}, expected from the transformer calculations using winding ratios

Fig 38. V_{CC} higher than anticipated due to ringing

Depending on the power consumption of the IC plus base drive and the power, delivered by the collector current of the NPN when switched off at the emitter, the rectified voltage of the auxiliary winding follows the average or the peak of the ringing (peak rectification).

Therefore, the supply voltage can be higher than anticipated. The amount of ringing is depending on the coupling of the auxiliary winding with the primary and secondary winding. It may be necessary to adapt the number of auxiliary windings to get the correct supply voltage.

The supply voltage range is rather large (8 V to 40 V). For optimum efficiency and no-load input power design V_{CC} on 10 V to 12 V at no-load at the minimum V_{in} (85 V (AC)). Because the ringing and the charge, delivered by the collector current at switch-off increases for higher load, the supply rises to 20 V to 22 V at full load.

6.9 Load line compensation

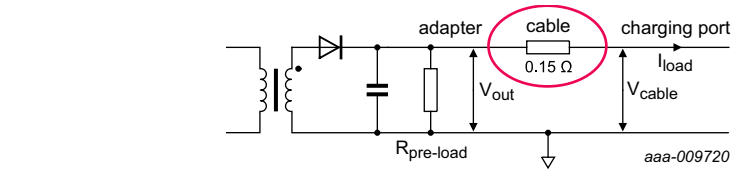
For a stable regulation, it is required that the voltage on the FB pin drops for higher loads. This leads to a load line from zero load to full load of 500 mV. The IC has a built-in load line compensation that limits the load line from zero to full load to 250 mV.

6.10 Cable compensation

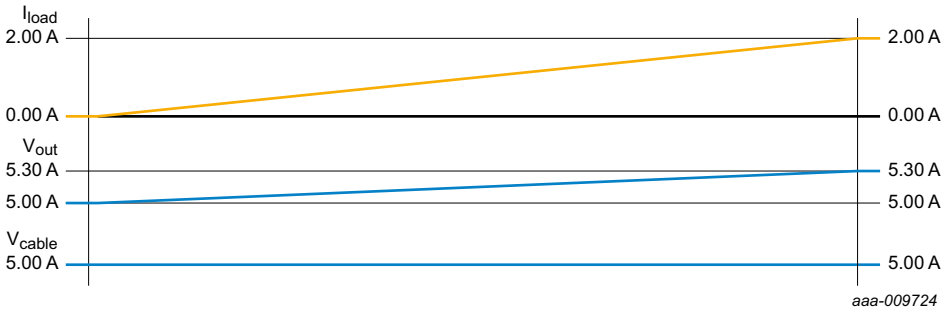
Standard cables with a specified fixed resistance are often used with smartphone chargers.

IC versions with cable compensation increase the output voltage (V_{out}) depending on the delivered output power to compensate the voltage drop over the cable.

Figure 39 shows the effect of cable compensation for a compensation voltage of 0.3 V.



a. Schematic



b. Waveform

Fig 39. Cable compensation

Cable compensation uses positive feedback. The regulation loop has to be slow to prevent instability. For load steps, an additional drop of the output voltage (V_{out}) at the end of the cable occurs because of the voltage drop over the cable.

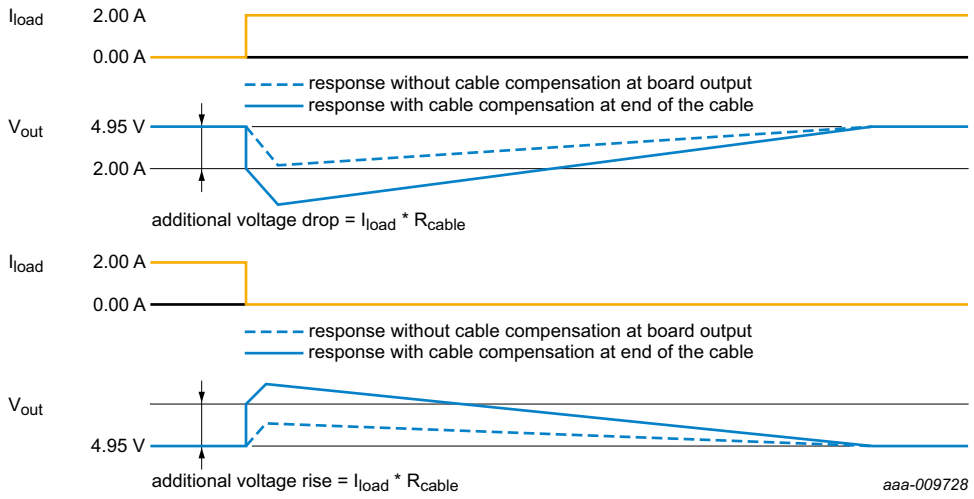


Fig 40. Additional voltage step due to cable compensation

The slow cable compensation loop causes an additional voltage step at the end of the cable of $I_{load} \times R_{cable}$ = cable compensation voltage both for positive as negative load steps.

When using cable compensation the output capacitors must to be enlarged to compensate for the extra voltage drop after a load step at the end of the cable.

Different cable compensation voltages are available (no compensation, 0.2 V, 0.3 V, 0.44 V).

6.11 Jitter

To improve ElectroMagnetic Interference (EMI), the switching frequency varies around the center value, resulting in reduced peak levels around the switching frequency. Jitter of approximately ±8 % is present in all modes. The jitter frequency is between 100 Hz and 400 Hz. To keep P_{out} constant while varying f_{sw}, I_{pk} is adapted accordingly as can be derived from Equation 16.

$$P_{out} = 0.5 \times L_p \times I_{pk}^{2} \times f_{sw} \times \eta \quad (16)$$

6.12 Protective features

The following protections are implemented:

- UnderVoltage Protection (UVP) on the VCC pin
- OverVoltage Protection (OVP) on V_{out} (via the FB pin)
- OverTemperature Protection (OTP)
- Demagnetization protection
- Open/short circuit protection on the FB pin
- Hiccup mode for overload/short circuit protection of the output
- Short circuit protection on the SENSE pin

6.12.1 Undervoltage protection on the VCC pin

The UVP on the VCC pin prevents unpredictable behavior when the supply voltage drops to below the minimum level required for operation. When the voltage on the VCC pin drops to below 8.5 V ($V_{CC(stop)}$) the IC restarts.

Restarting the IC causes switching to stop. The high-voltage current source is enabled to charge the VCC capacitor. When VCC exceeds 17 V ($V_{CC(startup)}$), the high-voltage current source is disabled and switching restarts.

If the error persists, the sequence repeats itself. This condition is known as the hiccup mode.

6.12.2 Overvoltage protection on V_{out}

The voltage on secondary side is monitored using V_{FB} (measured on the FB pin). During normal operation, $V_{FB} \approx 2.5$ V when sampled during the secondary stroke. If $V_{FB} > 3.2$ V, a forced restart is performed.

When the sampled voltage on pin FB > 3.2 V, switching stops. The auxiliary winding no longer provides the VCC supply and V_{CC} drops. If required, the IC waits until the VCC supply < 8.5 V before enabling the high-voltage current source to charge the VCC capacitor.

When $V_{CC(startup)} > 17$ V, the high-voltage current source is switched off and the switching is reenabled. If the error persists and the sampled voltage on pin FB exceeds 3.2 V, switching stops, the sequence repeats itself. This condition is known as the hiccup mode.

The overvoltage level is determined as follows:

- Sampled voltage on the FB pin for V_{out} = 5 V: 2.5 V
- The voltage on the secondary winding before the diode: 5.3 V
- The secondary winding voltage ratio divided by the sampled voltage on the FB pin is 5.3 V / 2.5 V = 2.12
- The secondary winding voltage at a sampled voltage on the FB pin of 3.2 V: 3.2 V $\times$ 2.12 = 6.8 V
- V_{out} after the diode becomes: 6.8 V – 0.3 V = 6.5 V

The output voltage must exceed 6.5 V before OVP is triggered. In practice, OVP triggers when the output voltage is between 6.5 V and 6.8 V, depending on the steepness of the V_{out} increase.

6.12.3 Overtemperature protection

When the temperature of the IC exceeds 150 °C, OTP is activated. The IC stops switching and V_{CC} drops. When V_{CC} drops to below $V_{CC(stop)}$ (8.5 V), the high-voltage current source charges the VCC capacitor until 17 V ($V_{CC(startup)}$) is reached. The IC does not start switching until the die temperature drops to below 100 °C. During the waiting time, V_{CC} cycles between charging to $V_{CC(startup)}$ and discharging of the non-switching TEA1720 to $V_{CC(stop)}$ by the quiescent current.

The hysteresis from 150 °C to 100 °C ensures that no dangerous situations occur.

6.12.4 Demagnetization protection

Demagnetization protection is implemented to check that the secondary stroke has ended before enabling the next primary stroke. This condition ensures discontinuous operation. It prevents stress in overload conditions.

Demagnetization monitors the level on the FB pin after the secondary stroke is started. The level must drop to below 50 mV before the next primary stroke is allowed. When no demagnetization is detected at the start of the next primary stroke, this stroke is skipped and the controller retries at the next primary stroke (cycle skipping).

6.12.5 Open/short protection on the FB pin

The FB pin detects if an AC voltage is present on the pin. When the voltage on the pin does not alternate below and above 50 mV, indicating the pin is not connected to the resistive feedback divider but open or shorted to ground, switching stops. Consequently, VCC drops to below $V_{CC(stop)}$ and the IC restarts. When VCC reaches 17 V ($V_{CC(startup)}$) at the first stroke, the level at the FB pin is checked again to see if it alternates below and above 50 mV. If not, the sequence repeats (hiccup mode). This action prevents the presence of an uncontrolled output voltage when the FB pin is open or shorted to ground.

6.12.6 Hiccup mode for overload/short circuit protection of the output

To limit the input power in case of overload and/or short circuit, the controller enters hiccup mode when V_{out} becomes too low.

The V_{out} level is monitored by the FB pin. When due to overload or a short circuit the sampled voltage on the FB pin drops to below 1.10 V ($V_{th(hiccup)}$) for longer than 20.9 ms ($t_{blank(hiccup)}$), the switching stops and the IC restarts.

When during a restart the sampled voltage on the FB pin does not exceed 1.40 V ($V_{th(rel)(hiccup)}$) within 20.9 ms ($t_{blank(hiccup)}$), the sequence is repeated until the fault condition is removed. When the fault condition is removed, normal operation is resumed.

Table 8 show the two levels for $V_{th(hiccup)}$.

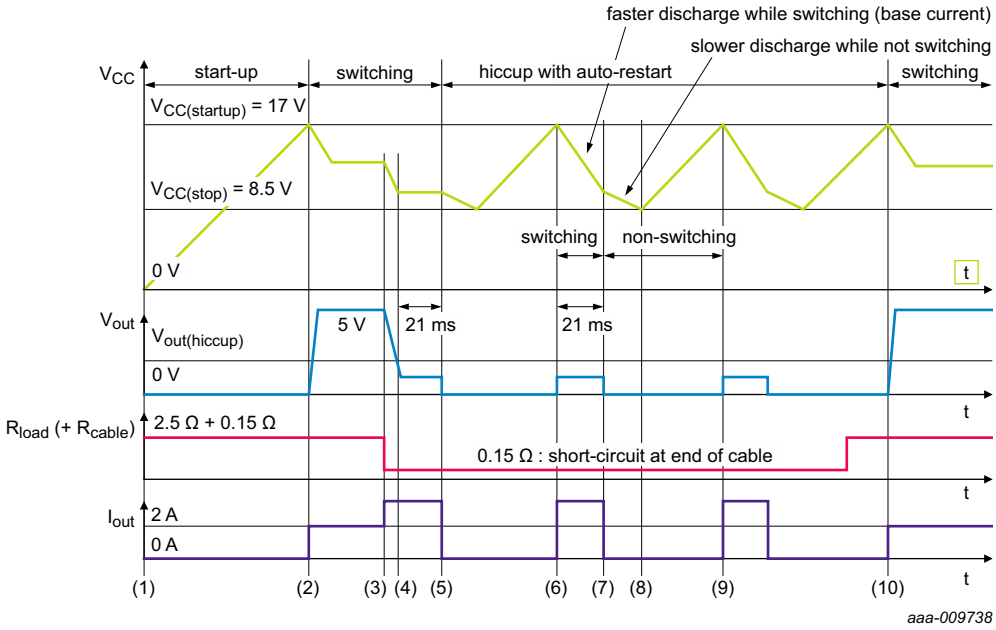
Table 8. Overview hiccup levels

Version	$V_{th(hiccup)}$	$V_{out(hiccup)}$	$V_{th(rel)(hiccup)}$	$V_{out(rel)}$	$t_{blank(hiccup)}$
1. USB standard	1.10 V	2.00 V	1.40 V	2.7 V	20.9 ms
2	1.47 V	2.7 V	1.70 V	3.1 V	20.9 ms

The values of $V_{out(hiccup)}$ and $V_{out(rel)}$ are given as guideline. The exact value depends on the used divider for the FB pin.

The first version is USB compliant (V_{out} remains in regulation until 2 V before the protection starts). The second version is meant for those who prefer protection to come in early.

The sequence is explained in the picture below.



(1) High-voltage current source charges VCC capacitor until $V_{CC(startup)}$ is reached.

(2) Switching starts. V_{out} rises to 5 V; I_{load} = 2 A.

(3) Short circuit occurs at end of the cable. I_{load} exceeds the Constant Current (CC) level. V_{out} drops to below $V_{out(hiccup)}$. V_{CC} also drops (V_{CC} is proportional to V_{out}).

(4) Switching continues for 20.9 ms ($t_{blank(hiccup)}$)

(5) After 20.9 ms, switching stops. V_{CC} drops to 8.5 V ($V_{CC(stop)}$). The hig-voltage current source is enabled and charges the VCC capacitor to 17 V ($V_{CC(startup)}$).The high-voltage current source is switched off.

(6) Switching starts. Due to the short, V_{out} does not exceed $V_{out(rel)}$. Switching continues for 20.9 ms ($t_{blank(hiccup)}$).

(7) After 20.9 ms, switching stops. The drop of V_{CC} continues but more slowly, because only the quiescent current for the TEA1720 is drawn (no base current).

(8) V_{CC} drops until 8.5 V ($V_{CC(stop)}$) is reached. The VCC capacitor is recharged.

(9) When V_{CC} reaches 17 V ($V_{CC(startup)}$) the sequence is repeated.

(10) When the short circuit is removed and switching starts, V_{out} will rise to exceed $V_{out(rel)}$ within 20.9 ms ($t_{blank(hiccup)}$). Normal operation is resumed.

Fig 41. Hiccup mode

The protection works the same for both overload and short circuit.

The input power P_{in} during protection is depending on the ratio between the time the IC is switching ($t_{blank(hiccup)}$) and the time no switching occurs (the VCC capacitor charging time, with roughly 1 mA from 8.5 V ($V_{CC(stop)}$) to 17 V ($V_{CC(startup)}$), and the time VCC drops after switching has stopped; see (6) to (9) in Figure 41). The charge time for a 10 µF VCC

capacitor is approximately:

$$VCC\ capacitor \times \left(\frac{(V_{CC(startup)} - V_{CC(stop)})}{I_{CC(startup)}}\right) = 10^{-5} \times \frac{(17 - 8.5)}{1.2^{-3}} = 71\ ms \quad (17)$$

To keep P_{in} for a 10 W charger below 1 W, a VCC capacitor of 10 µF is required. When the input power is too high, the VCC capacitor can be increased until the required input power is met.

Remark: The actual value of ceramic capacitors of that size (10 µF at 50 V) is often much lower when used at a 20 V supply voltage. The lower capacitance value causes P_{in} to increase.

6.12.7 Short circuit protection on the SENSE pin

The TEA1720 has a built-in protection for faults, caused by a short circuit of the SENSE pin to ground or a shorted R_{SENSE} resistor.

From the start of the primary stroke the voltage level on the SENSE pin is monitored. If the level has not increased to 125 mV ($V_{scp(high)}$) within 1.35 µs ($t_{blank(scp)SENSE}$), a short circuit is suspected and switching is stopped. V_{CC} drops to 8.5 V ($V_{CC(stop)}$) and the IC restarts. If the fault condition persists, the sequence is repeated (hiccup mode). Once the fault condition is removed, the IC restarts and normal operation is resumed.

The steepness of the primary current increase depends on the mains voltage. To compensate for the steepness variation, $t_{blank(scp)SENSE}$ is adapted according the mains voltage.

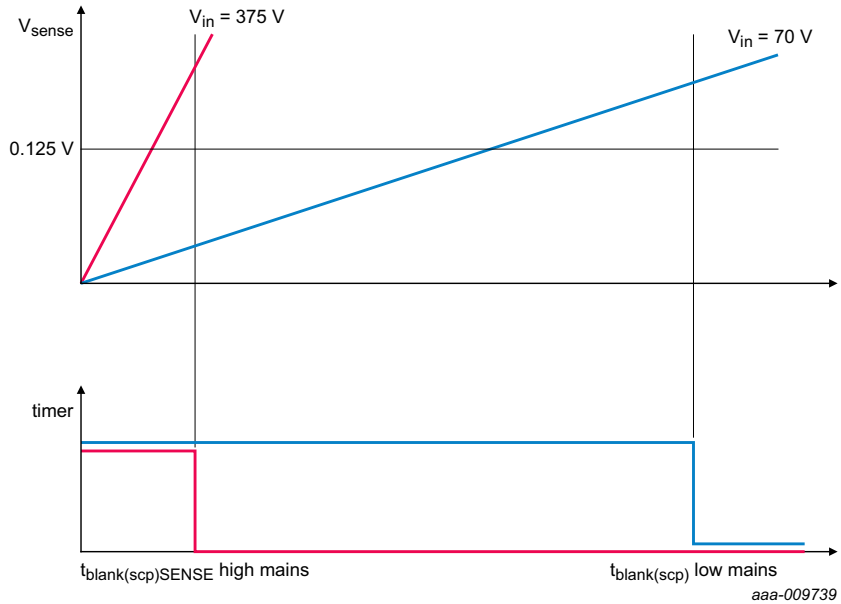


Fig 42. Short circuit protection on the SENSE pin; adaptive $t_{blank(scp)SENSE}$

V_{in} is the rectified mains voltage. The higher V_{mains} (and V_{in}), the shorter $t_{blank(scp)SENSE}$.

An additional protection is implemented when the short circuit on the SENSE pin occurs after the level of the SENSE pin passed 125 mV.

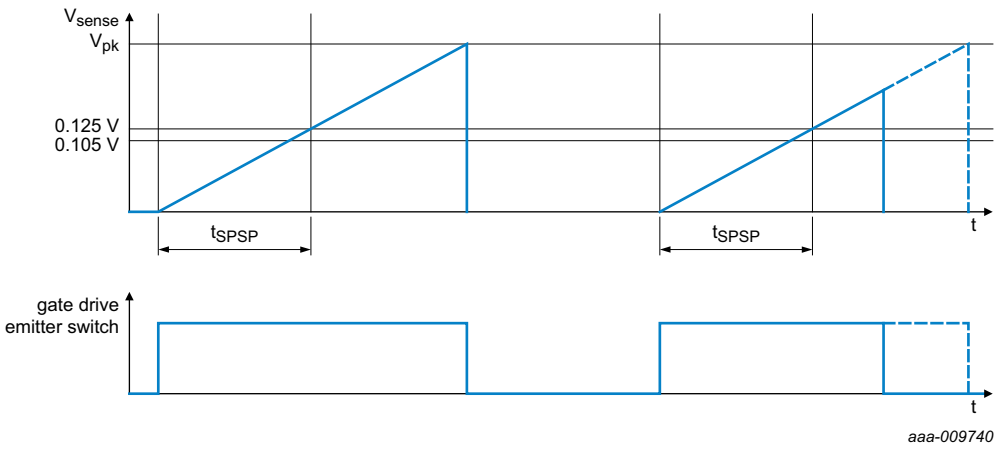


Fig 43. Short circuit protection on the SENSE pin for V_{sense} > 125 mV

The left hand side shows a normal stroke. V_{sense} exceeds 125 mV ($V_{scp(high)}$) within the required time ($t_{blank(scp)SENSE}$). The level on the SENSE pin reaches V_{pk} and the gate drive of the emitter switch is switched off.

At the next stroke V_{sense} exceeds 125 mV within $t_{blank(scp)SENSE}$ as well, but now a short circuit occurs before V_{pk} is reached. The voltage on the SENSE pin drops to below 105 mV ($V_{scp(low)}$). The gate drive immediately switches off. The hysteresis between the two detection levels (125 mV ($V_{scp(high)}$) and 105 mV ($V_{scp(low)}$) ensures stable behavior.

The conditions for SENSE pin short protection are listed below. The protection is only triggered when the following criteria are all met:

- The gate drive must still be active
- $t_{blank(scp)SENSE}$ has passed
- The V_{sense} level is still below 125 mV ($V_{scp(high)}$)

or

- The gate drive is still active
- $t_{blank(scp)SENSE}$ has passed
- The V_{sense} level drops to below 105 mV ($V_{scp(low)}$)

6.12.8 Protection overview table

Table 9. Overview protections

Protection	Level	Action
UVP on pin VCC (UnderVoltage LockOut (UVLO))	8.5 V ($V_{CC(stop)}$)	stop switching; restart
OVP on output voltage (V_{out})	V_{FB} > 3.2 V	stop switching; restart
OTP	die temperature > 150	stop switching until T < 100 °C
demagnetization	V_{FB} < 50 mV	hold next primary stroke until demagnetization has occurred
short/open circuit protection on the FB pin	AC detection on the FB pin	stop switching; restart
hiccup mode	V_{FB} < 1.1 V or V_{FB} < 1.47 V	Continues operation for 20.9 ms. If the condition still exists, stops switching, restarts. Otherwise the timer resets and operation is continued.
short circuit protection on the SENSE pin	V_{sense} < 125 mV at t < $t_{blank(scp)SENSE}$	stop switching; restart

7. Application

This chapter describes the following topics:

- Application diagram
- Transformer considerations
- ElectroMagnetic Interference (EMI)
- Tolerances

7.1 Application diagram

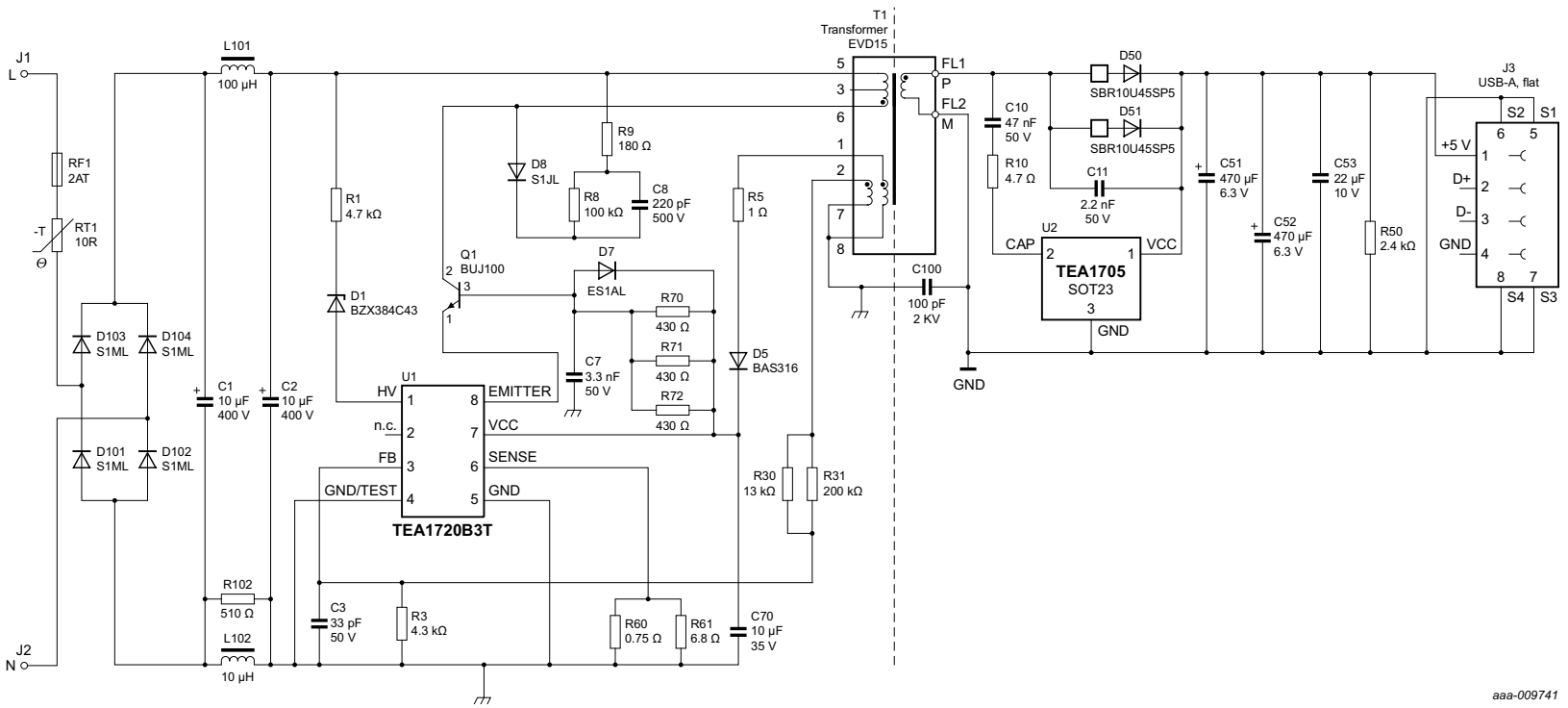


Fig 44. Schematic demo board

For the schematic, a 10 W charger application has been used. The following sections describe the various components, going from the AC input to the output.

7.1.1 Input part and EMI filter

RF1 is a 2 A fuse for short circuit protection on the primary side. The inrush current is limited by RT1, a 10 Ω NTC resistor. Using an NTC on this position limits the efficiency loss due to the series resistance.

For mains rectification, standard diodes are used. However using a diode bridge is also possible.

Capacitors C1 and C2 form the main electrolytic capacitor. Capacitors C1 and C2, inductors L101, L102, and resistor R102 form a damping filter for conducted EMI.

7.1.2 Connecting pin HV to the bus voltage

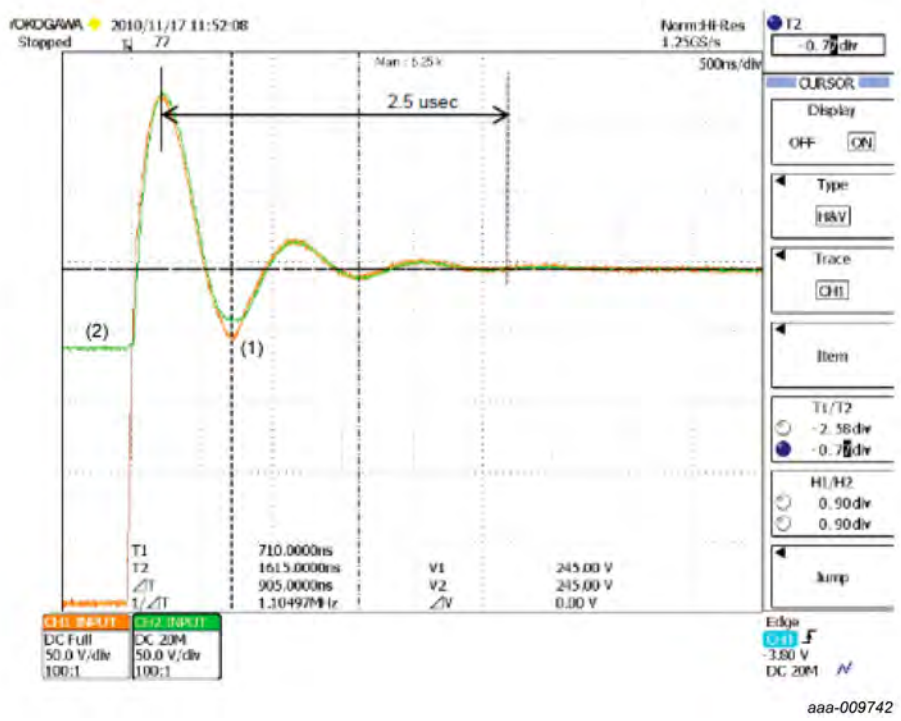
The HV pin of the TEA1720 is connected via resistor R1 and zener diode D1 to the rectified mains voltage. Resistor R1 is added to increase the protection for surge tests.

Zener diode D1 prevents a restart after disconnecting the charger from the mains at high input voltage and full load. In this condition, the voltage on the VCC capacitor drops to below 8.5 V ($V_{CC(stop)}$) while the mains electrolytic capacitors are only discharged to 50 V. The remaining 50 V is high enough to enable audible repetitive restarts of the TEA1720 via the HV pin.

To disable the restart option via the HV pin, the voltage must be lower than 20 V. The applied zener of 43 V in series together with the HV pin fulfills this requirement for voltages on the electrolytic capacitors up to 63 V. Tests show that zener values between 36 V and 75 V prevent the repetitive restarts and enable start-ups from 75 V (AC).

7.1.3 Clamp

Diode D8, resistors R8 and R9, and capacitor C8 are designed to dampen the ringing after switch-off of the NPN switch. D8 must be a slow diode for ringing damping. Figure 45 and Figure 46 show damping using a fast and a slow diode.

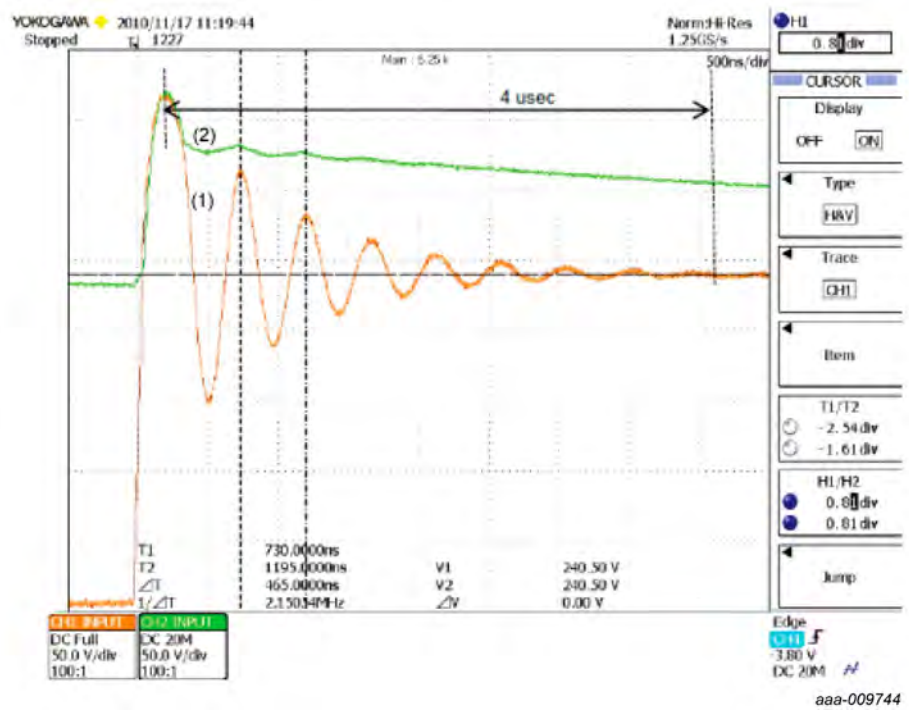


(1) Drain primary switch

(2) Cathode clamp diode

Fig 45. Damping using a slow diode (S1JL)

When using a slow diode, the diode conducts after the drain signal reaches its peak. The clamping circuit remains parallel to the primary. This action leads to the fast damping of the ringing. The ringing frequency is 1.1 MHz. The damping time is 2 μs.



(1) Drain primary switch

(2) Cathode clamp diode

Fig 46. Damping using fast diode (BYW26CV)

Using a fast diode, the clamping capacitor remains charged after reaching a peak. The clamping circuit is not active and does not provide further damping. The oscillation frequency is 2.2 MHz. The damping time increases to 4 μs. Quick damping of the oscillation is important to ensure proper measurement of the voltage on the FB pin at the end of the secondary stroke.

The value of R9 controls the damping. It is a compromise of damping speed and additional dissipation of the clamp. The values shown are a good starting point for a 10 W application.

7.1.4 Sense resistor

The sense resistor between the SENSE pin and ground incorporates two SMD resistors in parallel. Parallel configuration allows the use of standard SMD resistors for accurate tuning.

Tune the value of the source resistor in the real application. Exact calculation is hardly possible because of the influence of the used NPN switch (base current setting, storage time) on the actual $I_{pk(p)max}$ reached in the primary of the transformer.

For a first indication, the assumption is that the base current in the sense resistor compensates the increase of the collector current at switch-off. R_{sense} can be calculated with :

$$R_{sense} = \frac{V_{sense(pk)max}}{I_{pk(p)max}} \quad (18)$$

$V_{SENSE(pk)max}$ = 0.530 V. $I_{pk(p)max}$ is the peak current required to deliver full power as in the following calculation:

$P_{in(max)} = 0.5 \times L_p \times I_{pk(max)}^2 \times f_{max}$, where $P_{in(max)} = P_{out(max)} / \eta$, and η = 80 % for 10 W.

In practice, R_{sense} can deviate due to the difference between the base current and the increase of the collector current after switch-off of the NPN.

7.1.5 Auxiliary winding: Supply

One auxiliary winding of the transformer supplies the IC VCC voltage via R5, D5 and C70. The actual VCC level is depending on:

- The amount of ringing on the winding, which is related to the I_{pk} level and the coupling of the auxiliary winding to the primary. Ringing can cause the resulting VCC to be higher than the average level during secondary stroke.
- Charge by the collector current flowing via D7 when the emitter of the NPN is switched off. This additional charging increases for higher input voltages.

Check that V_{CC} remains above 8.5 V ($V_{CC(stop)}$) until V_{out} reaches 2.0 V or 2.7 V ($V_{out(hiccup)}$). Resistor R5 is added to prevent a short load of the auxiliary winding under no-load conditions that is too high. A short load can disturb the waveform at the FB pin.

The value of C70 must be at least 10 μF because it also supplies the base current from the NPN switch.

Remark: Install capacitor C70 as close to the IC as possible to suppress disturbances.

7.1.6 Base drive NPN

The supply voltage (V_{CC}) also provides the base drive of the NPN.

When the internal MOSFET of the TEA1720 switches on, the emitter of the NPN is pulled low. Capacitor C7 delivers the base charge at switch-on (NXP patent, patent pending). The base resistor which determines the sustaining base drive during on-time, is split into three parallel resistors (R70, R71 and R72) to handle the dissipation and the temperature.

Switching off the internal MOSFET directs the collector current through the base of the NPN which charges the VCC capacitor (C70) via diode D5.

To ensure the emitter current is always high enough to reach the maximum V_{pk} (530 mV), it is important that the sustaining base current is high enough.

Tests have shown that this condition is the most critical at low temperatures. The base drive must be checked at the minimal operation temperature with minimal VCC (8.5 V ($V_{CC(stop)}$); see Section 6.3.5).

7.1.7 Auxiliary winding: Feedback

To minimize disturbance on the signal for the FB pin, a separate auxiliary winding with a maximum coupling to the secondary winding is used for feedback. The resistive divider consists of resistors R3, R30, R31. Using two resistors in parallel enables the setting of an accurate division factor. Capacitor C3 is added for spike suppression.

Remark: Capacitor C3 must not be too large, because it disturbs the waveform at the FB pin and no accurate sampling of the voltage is possible. A value of 33 pF close to the pin is a good value to use.

7.1.8 Secondary side

To improve efficiency, two Schottky diodes (D50 and D51) are used in parallel for rectification on the secondary side,. Despite a 2 A rated output current, the peak current can be higher than 9 A. The diodes must be capable to handle a current higher than 9 A.

From rating point of view one diode can handle the current, but in that case, check the efficiency and the temperature of the diode. Capacitor C11 improves efficiency by starting an immediate conduction at the start of the secondary stroke.

To avoid disturbance by switching spikes, connect the VCC and GND of the transient controller TEA1705 as close as possible to the output. Capacitor C10 carries the charge to generate the wake-up pulse. Resistor R10 limits the charge current to safe values. For both components we applied 0603 parts successfully.

The output capacitors C51 and C52 manage the output ripple in burst mode at full load. For the output ripple and load step behavior, use capacitors with low Equivalent Series Resistance (ESR) like aluminum polymer electrolytic capacitors. Capacitor C53, a ceramic capacitor of 22 μF, is added for improved switching spike suppression.

Resistor R50 is the preload resistor. It serves two purposes:

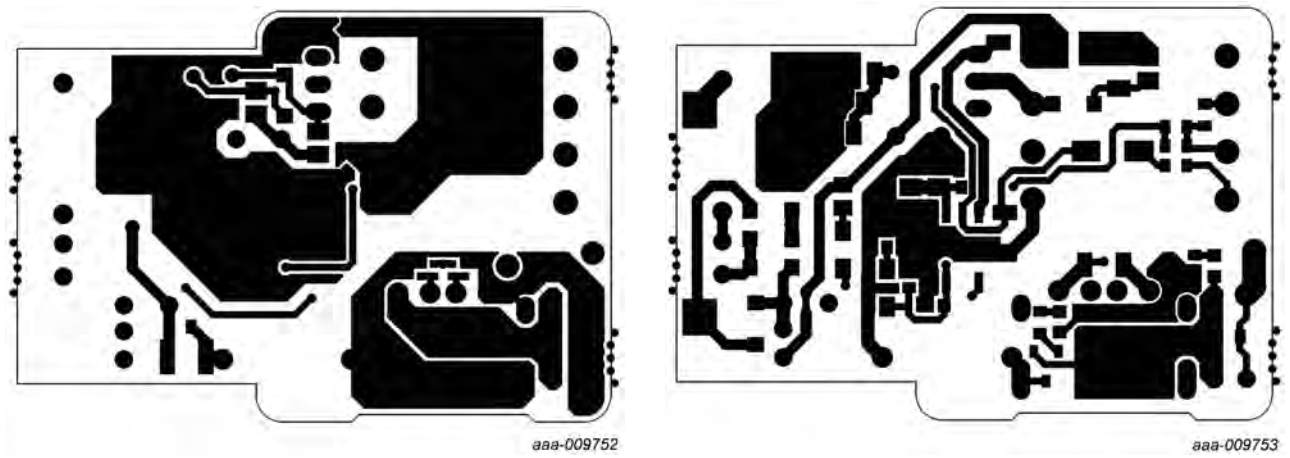
- A small load on the secondary side ensures proper regulation of the output voltage at a no-load condition.
- The preload resistor dissipates any excess of energy above the IC supply, base current of the NPN switch, and the auxiliary divider generated in a no-load condition by the fixed burst frequency and fixed I_{pk}. If excess energy is not dissipated, the output voltage increases to the OVP level.

7.2 Layout considerations

A careful layout of the board is important to enable stable behavior under all conditions and to meet the input/output, EMC, and thermal requirements. For the best result the following items should be taken into account:

- Small power current loops to achieve a low radiated EMI level
- Separation of large and small signal path
- Secondary side routing to optimize ripple and noise
- Routing input filter part
- Thermal considerations

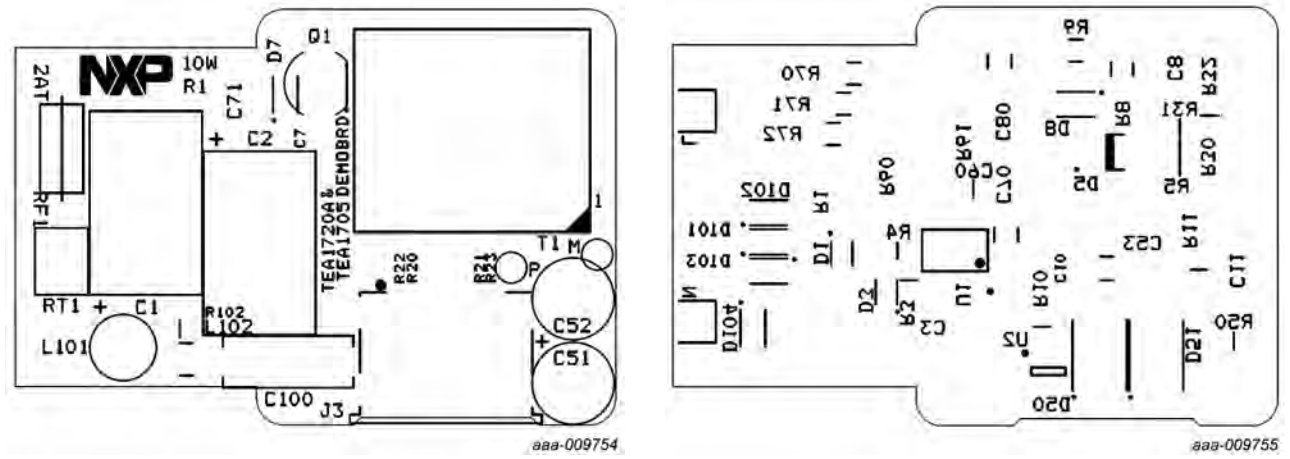
Figure 47 to Figure 49 show the layout of the demo board. Figure 44 shows schematic diagram.



a. Top

b. Bottom

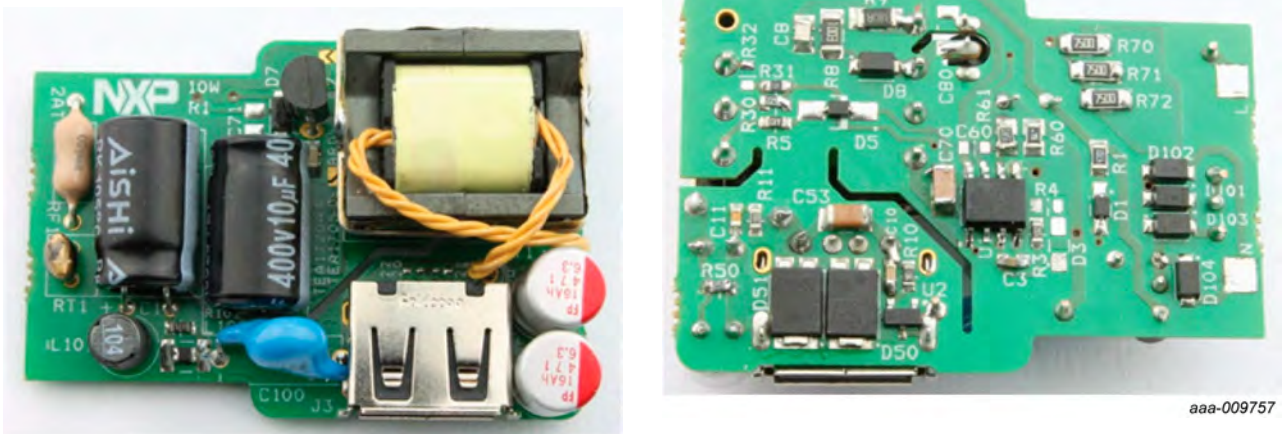
Fig 47. Copper



a. Top

b. Bottom

Fig 48. Silk screen



a. Top

b. Bottom

Fig 49. Demo board

7.2.1 Small power current loops to achieve a low radiated EMI level

To achieve a low radiated EMI level, the loop surface areas of the main power current loops must be kept as small as possible during the primary and the secondary stroke. At switch-off of the NPN and switch-on of the diodes D50 and D51 high dI/dt's are present at the main current loops. Those dI/dt's induce Electromagnetic fields in these power current loops. This can cause radiated EMI when the loop surface areas are too large.

During the primary stroke, the power current flows from the + terminal of capacitor C2 through the primary winding, the NPN, the IC internal emitter switch, and the current sense resistors, back to the ground of capacitor C2 (the star ground). To keep the surface area of this current loop small, place the peak-clamp outside the main current loop.

During the secondary stroke, the power current flows from the transformer winding (FL1) through the output diodes (D50 and D51) to the output capacitors C51 and C52 and back to the transformer winding (FL2).

Always keep the loop surface area of the peak-clamp as small as possible. The charge current of peak clamp flows from the transformer collector connection (pin 6 of the tranformer; see Figure 44 for the transformer pin arrangement) through the diode D8, resistor R9 and capacitor C8 back to transformer bus voltage connection (pin 5 of the transformer; see Figure 44 for the transformer pin arrangement).

7.2.2 Separation of large and small signal path

The ground connection of bulk electrolytic capacitor C2 acts as star ground. Here all grounds (large signal, small signal) come together.

Connect all power grounds with a star grounding pattern to the ground connection of capacitor C2.

Connect all small signal grounds with a star grounding pattern to the IC GND pins. Connect the two IC GND pins together at the PCB with a PCB trace that is as short as possible.

The PCB trace between the IC GND pins and the ground connection of capacitor C2 must be as short and as wide as possible.

At switch-off of the NPN a steeply increasing voltage with a high dV/dt is present at the collector connection (pin 6 of the transformer; see Figure 44 for the transformer pin arrangement) of the transformer. This dV/dt causes a capacitive current to flow from the primary winding to the auxilliary winding or the shield in the transformer, connected to the transformer auxilliary winding ground (pin 7 and 8 of the transformer; see Figure 44 for the transformer pin arrangement). This current flows from the transformer winding ground to the IC ground. From the IC ground it flows to the ground connection of the bulk electrolytic capacitor C2, through the current sense resistors (R60 and R61) and the parasitic capacitance of the NPN back to the transformer. This current may disturb the small signal measurements of the IC. Use the IC ground as star ground for the small signals and the parasitic current in the auxilliary winding ground.

Place resistors R3, R30, R31 and capacitor C3, connected to the IC FB pin, as close as possible to the IC to avoid that power current loops, mains transients, and ESD events disturb the FB pin.

At the secondary side, connect Y-cap C100 as close as possible to the USB-A metal frame (S1 to S4). At the primary side, connect Y-cap C100 as close as possible to the anodes of bridge rectifier diodes D101 and D102.

When using ground planes, in case of double layer board, connect them to the power or small signal star ground at one point only.

7.2.3 Secondary side routing to optimize ripple and noise

To divide the current distribution through both diodes equally, design the layout as symmetrical as possible, when using two diodes at the output.

To minimize the output ripple and noise, a proper PCB trace from the cathode of diodes D50/D51 to the USB-A (J3) +5 V and from transformer ground (T1 FL2) to the USB-A (J3) GND is required. Trace the PCB from the cathode of D50/D51 to the + connection of capacitor C51 first, then to the + connection of capacitor C52, and finally to the USB +5 V.

Trace the transformer ground must to the ground connection of capacitor C51 first, then to the ground connection of capacitor C52, and finally to the USB-A GND. Place capacitor C53 as close as possible to the USB connector. Capacitor C11 is added to suppress switching spikes. The position of preload resistor R50 is not critical.

7.2.4 Organizing the input part

The input part is organized so that interference from switching cannot reach the mains connection without passing through the filter L1, L2 and C1. Create enough distance so that crosstalk directly to the mains connections is avoided.

7.2.5 Thermal considerations

Make sure that in this application the component temperatures do not exceed requirements. Most critical components are the NPN, the output diodes and the NPN base resistors. If the NPN case temperature is higher than the transformer core temperature, the NPN can be glued to the transformer with thermal compound.

Because of the dissipation in the output diodes (D50, D51) and the base resistors (R70, R71 and R72), place them at a copper area of sufficient size. In the demo board three 1206 base resistors are placed in parallel to keep the temperature of every single resistor within the requirements. Provide as much copper area as possible at the diode connections and base resistor connections for cooling. When using a double sided PCB, put copper areas at both sides of the PCB, thermally connected using via's.

7.3 Transformer

A proper construction of the transformer is required for the primary sensing concept.

Topics are:

- L_p and I_{pk} in relation to input voltage and power
- For proper V_{out} sampling, the secondary stroke must be long enough
- Transformer construction of windings
- Safety

This chapter describes the basics, including the calculation of the main parameters which can be used when dealing with a transformer manufacturer.

7.3.1 Calculating L_p and I_{pk}

Table 10 shows a calculation example for a 10 W application.

Only the main items, which determine the transformer are calculated, the primary inductance $_{Lp}$ and the peak current I_{pk} at maximum output power.

Table 10. Calculation L_p and I_{pk}

Definition	Values	Unit	Description
Values depending on design			
V_O	5.00	V (DC)	output voltage converter at maximum load (at PCB end)
$I_{o(max)}$	2.20	A	maximum output current at border of CV/CC mode
$V_{th(hiccup)}$	2.70	V	output voltage in CC mode where the hiccup/safe restart is entered
$V_{F(sec)}$	0.40	V	forward voltage secondary diode (Schottky)
C_{mains}	17.4	µF	total bulk electrolytic capacitor value. Use approximately 2 µF per Watt output power (take into account the lower limit of the capacitor tolerance)
$V_{mains(min)}$	85	V (AC)	lowest specified mains input voltage for full performance
$V_{mains(max)}$	265	V (AC)	highest specified mains input voltage for full performance
f_{mains}	60	Hz	frequency mains voltage at $V_{mains(min)}$
nV_{out_select}	84	V	select the highest value for which $t_{sec(min)} \leq 1.9$ µs
η	0.77	-	converter efficiency at maximum load (= border of CV/CC mode) and $V_{mains(min)}$
Calculation of minimum DC voltage at the bulk electrolytic capacitor			

Table 10. Calculation L_p and I_{pk} *...continued*

Definition	Values	Unit	Description
P_{in}	14.29	W	$P_{in} = V_O * I_{O(max)} / \eta$
$V_{pk(elcap)}$	118.81	V	$V_{pk(elcap)} = V_{mains(min)} * \sqrt{2} - 2 *$ drop over mains rectifier diodes (0.7 V/diode)
$V_{min(elcap)}$	67.56	V	Vmin(elcap) is where the dropping voltage of the electrolytic capacitor meets the increasing mains voltage
Calculation $I_{pk(max)}$ and L_p			
$f_{osc(high)}$	54	kHz	data sheet value, maximum limit
$t_{dead(min)perc}$	0.02		$1 / f_{sw} = t_{prim} + t_{sec} + t_{dead(min)}$; $t_{dead(min)}$ to ensure discontinuous operation
$t_{dead(min)}$	370	ns	$t_{dead(min)} = 1 / f_{sw} * t_{dead(min)perc}$
$I_{pk(max)}$	0.779	A	$I_{pk(max)} = (2 * P_{in} * (V_{min(elcap)} + nV_{out})) / ((V_{min(elcap)} * nV_{out}) * (1 - t_{dead(min)perc}))$
$L_{p(max)}$	873	µH	$L_p = (1 / f_{osc(max)} - t_{dead(min)}) * 1 / (1 / V_{min(elcap)} + 1 / nV_{out}) * 1 / I_{pk(max)}$

The calculation is done using an Excel spreadsheet. The used equations are explained in the Description column of Table 10.

Remarks:

- The frequency, selected for the lowest mains, is 60 Hz. All 50 Hz mains have nominal voltages of 220 V or higher. It is not realistic these drop to 85 V.
- The value of nV_{out} (the output voltage multiplied by the ratio of the number of primary windings and number of secondary windings) influences two design parameters:
  - The peak voltage on the primary switch
  - The secondary stroke time

The peak voltage on the primary switch when switched off can be cacluated with Equation 19:

$$V_{pk(prim)} = V_{elcap(max)} + nV_{out} + V_{pk(ringing)} \quad (19)$$

Where:

- $V_{pk(prim)}$ must remain below the maximum breakdown voltage of the switch
- $V_{elcap(max)}$ is reached for the maximum AC input voltage (264 V (AC)). It is approximately 375 V (DC).
- $V_{pk(ringing)}$ can go up to approximately 100 V.

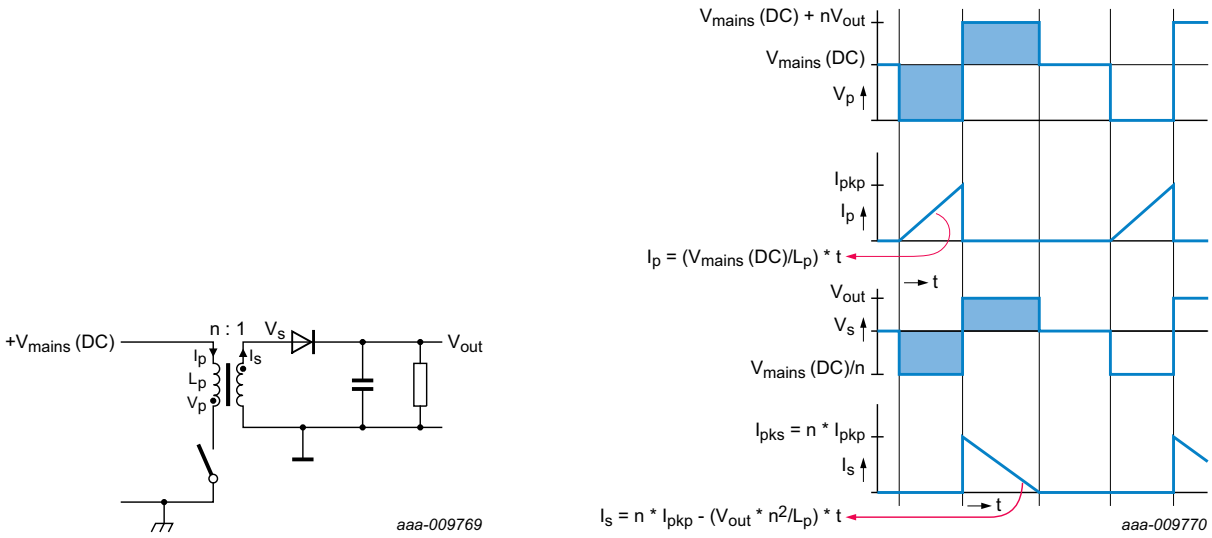
Using nV_{out} can keep $V_{pk(prim)}$ at safe levels.

7.3.2 Secondary stroke time

This section describes the relation between nV_{out} and the secondary stroke time.

The sampling time during the secondary stroke time and the secondary stroke time itself are related to the output power. The sampling timing must fit within the secondary stroke time.

Figure 50 shows some basic signals. they help understand the relation between the secondary stroke time and the transformer.



Condition: discontinuous conduction mode.

I_{pkp} = primary peak current; I_{pks} = secondary peak current.

Remark: Secondary diode drop is neglected.

a. Schematic

b. Waveform

Fig 50. Calculating the secondary stroke time

During primary stroke time, the primary peak current increases linearly with a slope of the DC voltage over the primary V_{DC} divided by the inductance L_p.

The current on secondary side (I_s) starts with the transformed current to the secondary side: $I_{pk(prim)} * n$. It decreases linearly to zero with a slope proportional to the output voltage V_{out}, and inversely proportional to Lp/n^2.

From the equation for the secondary current we can derive an equation for the secondary stroke time (t_s).

$$I_s = n \times I_{pkp} - \left(\frac{V_{out}}{\left(\frac{L_p}{n^2} \right)} \right) \times t \quad (20)$$

The secondary stroke time (t_s) is reached when I_s becomes zero:

$$t_s = L_p \times \frac{I_{pkp}}{(n \times V_{out})} \quad (21)$$

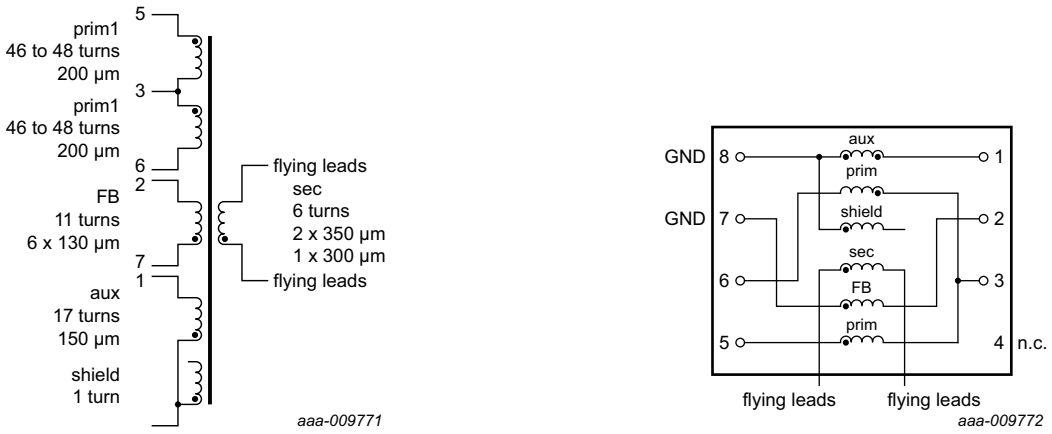
For correct sampling the minimum secondary stroke time ($t_{s(min)}$ for $I_{pk} = I_{pk(min)}$ is 1.9 µs.

The ratio between $I_{pk(min)}$ and $I_{pk(max)}$ is approximately 4.9.

When the calculated $t_{s(min)}$ is too short, the time can be increased by lowering nV_{out} in the calculation of Section 7.3.1 and recalculate L_p and I_{pk}.

7.3.3 Construction of windings

A suitable setup of the winding scheme as used in our demo board.



a. Schematic

b. Bottom view

Fig 51. EVD15 Transformer

The black dot shows the winding direction.

Fig 52. EVD15 construction and winding configuration

Table 11. Winding data

Layer number	Color	Winding	Wires parallel	Number of turns	Wire diameter
11	amber	aux winding	1	17	150 µm
10	purple	isolation tape			
9	blue	primary (sandwich)	1	46 to 48	200 µm
8	purple	isolation tape			
7	green	shield		1	
6	purple	isolation tape			

Table 11. Winding data *…continued*

Layer number	Color	Winding	Wires parallel	Number of turns	Wire diameter
5	yellow	secondary winding	3	6	2 × 350 μm TIW 1 × 300 μm TIW
4	purple	isolation tape			
3	red	FB winding	6	11	130 μm
2	purple	isolation tape			
1	blue	primary (sandwich)	1	46 to 48	200 μm

The primary inductance for a typical 10 W transformer is 880 μH. The secondary winding must be Triple Isolated Wire (TIW) to meet the safety standards.

7.3.4 Safety requirements

Because the output power is rather low, it is possible to use cores that are quite small for the transformer (EEM12.4 for 5 W; EVD15 for 10 W). With these transformer sizes, make sure that the safety requirements for mains isolation are met.

Using TIW for the secondary winding enables to keep the construction still small.

The pins of the bobbins for EE12.4 and EVD14 cores are often not spaced far enough apart to fulfill the safety distance between hot and cold. The only solution is to use flying leads to connect the secondary windings far enough from the primary pins at the bobbin. However, flying leads are not convenient for production.

Some bobbin manufacturers can supply bobbins with the required safety distances. These bobbins incorporate an extended secondary side footprint. They increase the footprint but ensure easy production.

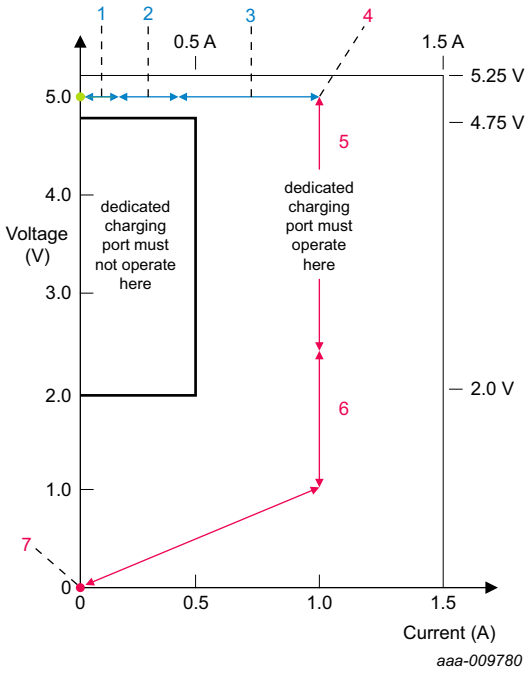
8. Appendix

8.1 USB specification

The TEA172X is designed to fulfill the USB specification for chargers. Currently, USB 1.1 is used. However, USB 1.2 is advancing. The most important requirements are described below.

8.1.1 USB 1.1

Figure 53 shows a graph of the static voltage versus current requirement for a USB 1.1 charger.



The graph is valid for a quasi-stationary load without jitter and without spread.

(1) CVB; burst mode with energy saving; no-load = 10 mW to low load = 120 mW.

(2) CVC: 120 mW up to 2 W.

(3) CVF: 2 W up to 5 W.

(4) CP: 5 W with transition from CV to CC.

(5) CCF: 5 W down to 2.5 W.

(6) CCC: Constant voltage with burst mode. 2.5 W down to 1 W.

(7) Start-up and UVLO. No power conversion.

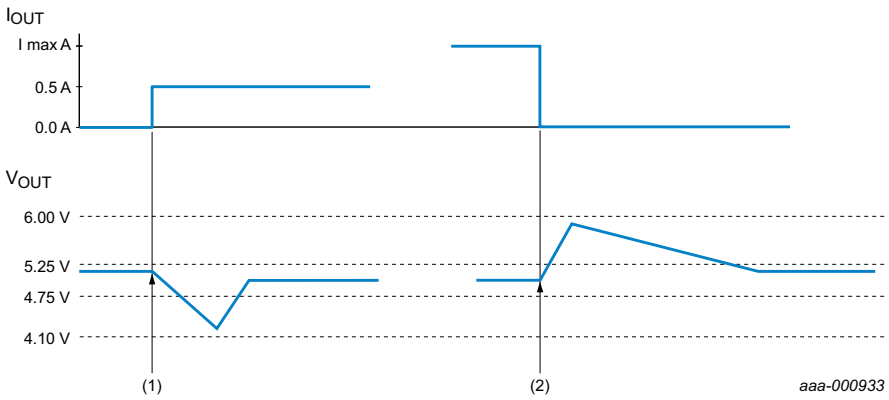
Fig 53. USB 1.1 static behavior and TEA172X operation modes

Figure 53 shows the voltage versus current for a 5 W USB charger using the TEA172X. The USB 1.1 specification requires precise voltage regulation (5 V ±5 % or 4.75 V to 5.25 V) and an output current up to 0.5 A. When higher than 0.5 A, the output current must remain between 0.5 A and 1.5 A. The output voltage must remain < 5.25 V.

If V_{out} drops to below 2 V, the power supply is allowed to shut down. It starts to "hiccup". The power supply can also continue to deliver current for as long as the output current remains < 1.5 A. The characteristic of most chargers is to keep the output voltage between 4.75 V and 5.25 V until maximum output power is reached. When maximum output power is reached, the chargers switch to current mode for charging.

The current mode has to work at least until an output voltage of 2 V is reached. When the output voltage is < 2 V, behavior is not critical unless the output current increases to exceed 1.5 A. For the USB 1.1 characteristic, the different operating modes of the TEA172X are indicated.

Figure 54 shows the dynamic behavior requirements of USB 1.1 for a 5 W charger.



(1) Load step 0 A ≥ 0.5 A. Requirements:
- V_{out} must remain > 4.1 V
- V_{out} average (over 1 s) must remain between 4.75 V and 5.25 V

No time limits for recovery.

(2) Load step I_{max} ≥ 0 A. Requirement:
- V_{out} must remain < 6 V
- V_{out} average (over 1 s) must remain between 4.75 V and 5.25 V

No time limit for recovery.

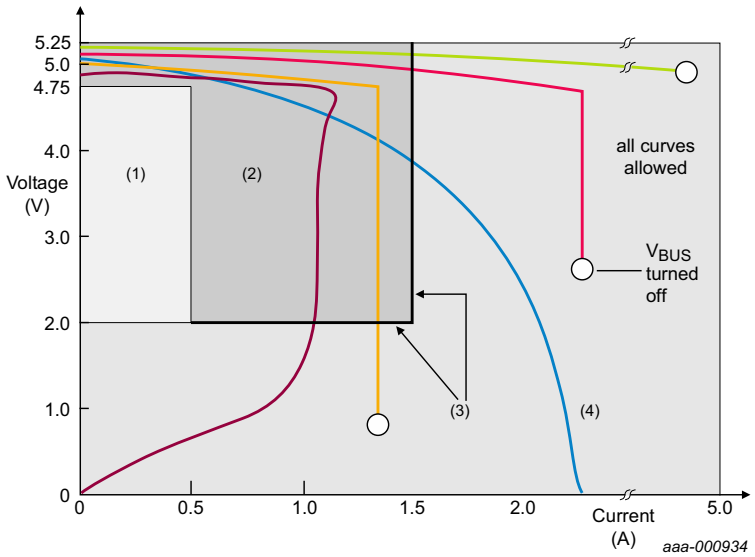
Fig 54. USB 1.1 dynamic behavior

For any load step between 0 A and 0.5 A, V_{out} must not drop to below 4.1 V. This requirement is used to calculate the size of the output capacitors.

For any load step between $I_{out(max)}$ and 0 A, the output voltage must not exceed 6 V. The output voltage must remain between 4.75 V and 5.25 V when averaged over 1 s.

8.1.2 USB 1.2

Figure 55 shows the static behavior for USB 1.2, which is less demanding on a number of aspects when compared to USB 1.1.



The specification for the output voltage remains narrow until the output current reaches 0.5 A (4.75 V to 5.25 V). No requirement for current limitation or minimal required V_{out} (V_{BUS}).

(1) Charging port operation not allowed.

(2) Required operating range for Dedicated Charging Port (DCP).

(3) Valid load curve must cross both lines.

(4) Continuous current regulation allowed. Current limit trip operation allowed.

Fig 55. USB 1.2 static behavior

The USB 1.2 specification is identical to USB 1.1 up to an 0.5 A output current. At 0.5 A, V_{out} must remain between 4.75 V and 5.25 V. When the output current exceeds 0.5 A, there are no requirements except that the output voltage must remain < 5.25 V and the output current must remain < 5 A.

At output currents < 1.5 A, the device must operate until the output voltage is 2 V. When the output voltage is < 2 V or the output current is > 1.5 A, the device can shut down, enter hiccup mode, or deliver any current < 5 A. In practice, most customers do not allow currents in this mode above the nominal charge current to avoid excessive dissipation.

A major relaxation of USB 1.2 related to dynamic behavior are load steps. Load steps have been divided into two ranges and three current levels. Table 12 shows an overview of the load steps.

Table 12. Load steps

I_{DCP}	Min	Max	Unit
low	0	0.03	A
mid	0.03	0.1	A
high	0.5	-	A

Load steps are divided into the three Dedicated Charging Port (DCP) current ranges:

- I_{DCP} low to I_{DCP} mid
- I_{DCP} mid to I_{DCP} high
- I_{DCP} low to I_{DCP} high

The additional I_{DCP} mid level allows a relaxation of the undershoot requirements for primary sensed chargers with low standby power, provided the USB device is designed for USB 1.2. Figure 56 shows the requirements for undershoot during current steps from low to mid and mid to high.

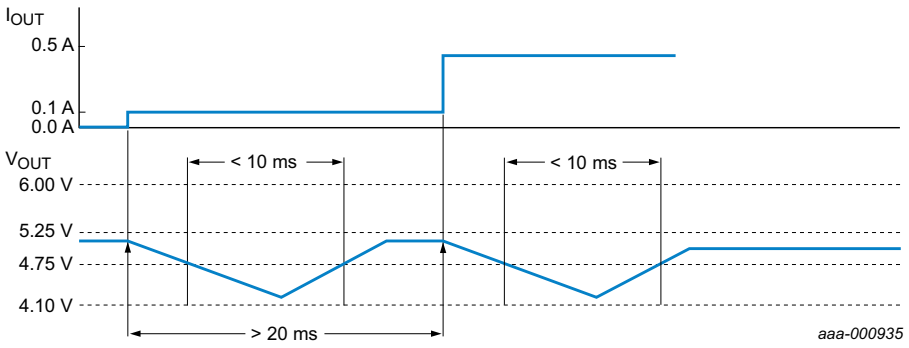
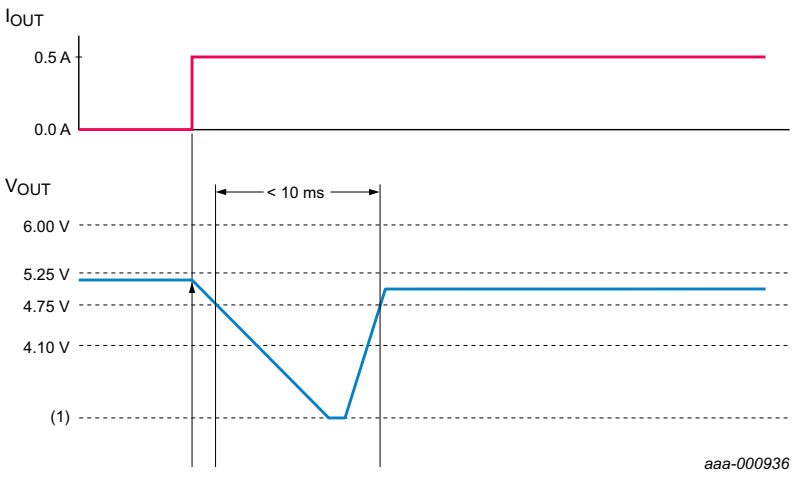


Fig 56. USB dynamic undershoot 1

For load steps from I_{DCP} low to I_{DCP} mid (0 A to 0.03 A and up to 0.10 A) and from I_{DCP} mid to I_{DCP} high (0.03 A to 0.10 A and up to 0.5 A), the following requirements apply:

- V_{out} must remain > 4.1 V
- The duration of the undershoot at V_{out} < 4.75 V must be < 10 ms
- The minimum time between load step 0 A to 0.03 A and up to 0.10 A and load step 0.03 A to 0.10 A and up to 0.5 A is 20 ms.

Figure 57 shows the requirements for undershoot during current steps from low to high.



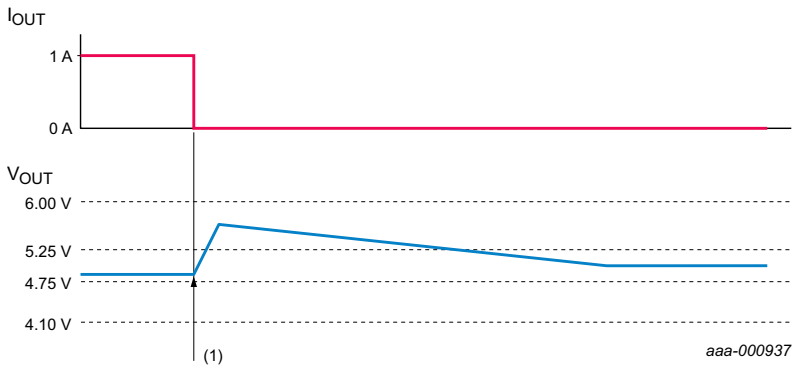
(1) Load voltage of attached PD (USB PD).

Fig 57. USB dynamic undershoot 2

For any load step between I_{DCP} low to I_{DCP} high (0 A to 0.03 A and up to 0.5 A) the following requirements apply:

- V_{out} can drop to the battery voltage of the attached Portable Device (PD)
- The undershoot (V_{out} < 4.75 V) must be < 10 ms

Figure 58 shows the requirement for load steps from high to low. They are the same requirements as for USB 1.1.



(1) Load step 1 A to 0 A (or any other load step down). Requirement, V_{out} must not exceed 6 V.

Fig 58. USB 1.2 dynamic overshoot

In general, the output voltage must not exceed 6 V for any load step during switch-on or during switch-off.

9. Abbreviations

Table 13. Abbreviations

Acronym	Description
USB	Universal Serial Bus
IC	Integrated circuit
BJT	Bipolar Junction Transistor
SMPS	Switched Mode Power Supply
EMI	ElectroMagnetic Interference
OVP	OverVoltage Protection
UVLO	UnderVoltage LockOut
OTP	OverTemperature Protection
PCB	Printed-Circuit Board
TIW	Triple Insulated Wire

10. Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits.

The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.

11. Contents

continued >>

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 5 December 2013
Document identifier: AN11401